

IN THE UNITED STATES DISTRICT COURT
FOR THE DISTRICT OF DELAWARE

POWER INTEGRATIONS, INC.,)	REDACTED
)	PUBLIC VERSION
Plaintiff,)	
)	
v.)	C.A. No. 04-1371-JJF
)	
FAIRCHILD SEMICONDUCTOR)	
INTERNATIONAL, INC., and FAIRCHILD)	
SEMICONDUCTOR CORPORATION,)	
)	
Defendants.)	

**COMBINED APPENDIX TO DEFENDANTS': (i) OPENING POST-TRIAL BRIEF
IN SUPPORT OF THEIR ASSERTION THAT THE PATENTS-IN-SUIT
ARE UNENFORCEABLE DUE TO INEQUITABLE CONDUCT; AND
(ii) PROPOSED FINDINGS OF FACT AND CONCLUSIONS OF LAW
REGARDING THE UNENFORCEABILITY OF THE PATENTS-IN-SUIT
DUE TO INEQUITABLE CONDUCT**

(VOLUME I of V)

ASHBY & GEDDES
Steven J. Balick (I.D. #2114)
John G. Day (I.D. #2403)
Lauren E. Maguire (I.D. #4261)
500 Delaware Avenue, 8th Floor
P.O. Box 1150
Wilmington, DE 19899
302-654-1888

Attorneys for Defendants

Of Counsel:

G. Hopkins Guy, III
Vickie L. Feeman
Bas de Blank
Brian H. VanderZanden
Orrick, Herrington & Sutcliffe LLP
1000 Marsh Road
Menlo Park, CA 94025
(650) 614-7400

Dated: November 5, 2007

TABLE OF CONTENTS

VOLUME I

DX 17, Electronic Design, Volume 38, No. 6 (March 22, 1990)

DX 55, International Electron Devices Meeting, December 5-7, 1983

DX 56, International Electron Devices Meeting, December 13-15, 1982

DX 59, Physics and Technology of Power MOSFETs, A Dissertation Submitted to the Department of Electrical Engineering and the Committee on Graduate Studies of Stanford University in Partial Fulfillment of the Requirements for the Degree of Doctor of Philosophy, Shi-Chung Sun (February 1982)

DX 69, Seventh Annual Applied Power Electronics Conference and Exposition, February 23-27, 1992

DX 70, PWR-SMP240, PWM Power Supply IC, 85-265 VAC Input, Isolated, Regulated DC Output

DX 74, PWR-SMP260, PWM Power Supply IC, 85-265 VAC Input, Isolated, Regulated DC Output

DX 76, SMP211, PWM Power Supply IC, 85-265 VAC Input, Isolated, Regulated DC Output

DX 77, PWR-SMP3, PWM Power Supply IC, 120 VAC Input, Isolated, Regulated DC Output

DX 89, United States Patent No. 4,626,879

DX 90, PIF 129750-129777

VOLUME II

DX 91, PIF 129301-129321

DX 100, Prosecution History, FCS0000015-114

DX 102, Prosecution History, FCS0000122-206

DX 104, Prosecution History, FCS0000226-316

DX 106, Prosecution History, FCS0000336-477

VOLUME III

DX 110, PIF17419

DX 113, Invention Disclosure Form, PIF 63314-24

DX 114, Project PS03 Index, 3/28/90, PIF 129325-46

DX 115, PIF 129387

DX 116, Project SMP1A Index, 3/27/90, PIF 129389-410

DX 117, PIF 129412-14

DX 118, PIF 129449-51

DX 119, PIF 129454-84

DX 120, SMP212/220 Task List, 8/14/92, PIF 129499-504

DX 121, PWR-SMP212, PWM Power Supply IC, 85-265 VAC Input, Isolated, Regulated DC Output

DX 122, PWR-SMP260, PWM Power Supply IC, 85-265 VAC Input, Isolated, Regulated DC Output

DX 123, PWR-SMP240, PWM Power Supply IC, 85-265 VAC Input, Isolated, Regulated DC Output

DX 124, PWR-SMP260, PWM Power Supply IC, 85-265 VAC Input, Isolated, Regulated DC Output

DX 125, PWR-SMP260, PWM Power Supply IC, 110/220 VAC Input, Isolated, Regulated DC Output

DX 126, PWR-SMP240, PWM Power Supply IC, 85-265 VAC Input, Isolated, Regulated DC Output

DX 192, United States Patent No. 5,146,298

DX 472, FCS1685956-93

DX 600, Optimum Design of Power MOSFETS, P.L. Hower, T.M.S. Heng and C. Huang, Unitrode Corporation, Watertown, Mass. 02171

DX 601, United States Patent & Trademark Office, Application No. 90/008,324

DX 602, United States Patent & Trademark Office, Application No. 90/008,327

DX 616, International Electron Devices Meeting, December 8-10, 1980

DX 617, International Solid-State Circuits Conference, February 18, 1981

DX 618, Process and Device Design of a 1000-Volt MOS IC

DX 619, Integrated Circuits for the Control of High Power, Robert S. Wrathall, David Tam, Louis Terry, Stephen P. Robb

DX 620, Integrated Power Devices, J. Tihanyi

DX 621, Journal of Solid-State Circuits, Vol. SC-15, No. 3, June 1980

DX 622, Integrated High and Low Voltage CMOS Technology

DX 623, International Solid-State Circuits Conference, February 18, 1981

DX 624, Lateral DMOS Transistor Optimized for High Voltage BIMOS Applications

DX 625, International Solid-State Circuits Conference, February 20, 1981

DX 626, Transactions on Electron Devices, FCS0526755-67

DX 627, High Voltage MOS Integrated Circuits, A Technology and Application Overview, KE001450-65

DX 628, KE001513-22

DX 629, KE001481-84

DX 633, Privilege Log for Klas Eklund documents

VOLUME IV

DX 1000, United States Patent No. 5,245,526

DX 1001, PWR-SMP211, PWM Power Supply IC, 85-265 VAC Input, Isolated, Regulated DC Output

DX 1002, PIF 129975-130008

DX 1003, Power Integrations' Responses and Objections to Defendants' Third Set of Requests for Admission (Nos. 44-50)

DX 1004, Form 10-Q, Filed 11/7/05 for Period Ending 9/30/05

DX 1005, International Electron Devices Meeting, December 3-5, 1979

DX 1006, Philips Journal of Research, Vol. 35, No. 1, March 13, 1980

DD1202

PX 1, United States Patent No. 6,249,879

PX 2, United States Patent No. 6,107,851

PX 3, United States Patent No. 6,229,366

PX 4, United States Patent No. 4,811,075

PX 8, PIF 00001-76

PX 19, Electronic Design, February 17, 1983, PIF 08765-70

PX 29, Klas Eklund notes

PX 30, Klas Eklund notes

PX 50, Letter to Alys Hay from Thomas Schatzel, KE 00012-14

PX 56, Technology License Agreement, PIF 23640-64

PX 272, 650V/1A, SPS 1-chip Process, FCS0176604-24

PX 325, Invention Disclosure Form, PIF 63306-13

PX 326, Invention Disclosure Form, PIF 63314-24

PX 412, KE001576-77

VOLUME V

Alex Djenguerian Deposition, 8/23/05

Klas Eklund Deposition, 10/14/05

Klas Eklund Deposition, 6/7/07

James Go Deposition, 9/14/05

Leif Lund Deposition, 8/15/05

Leif Lund Deposition, 3/2/06

Thomas Schatzel Deposition, 9/15/05

185623.1

DX 17

CHIPS SEND FULL-DUPLEX DATA, GRAPHICS
DETECTING SPEECH WITH NEURAL NETS

ENGINEERS AND ENGINEERING MANAGERS — WORLDWIDE

ELECTRONIC DESIGN

1215 ... Road
Windsor, Ontario

MAIL POSTE
Canada Post
Postage paid
Canada Canada
Post payé
Norte

A PENTON PUBLICATION U.S. \$5.00

MARCH 22, 1990

**SWITCHING
POWER
SUPPLIES
SUDDENLY
GET SMALLER**

CANADA INSTITUTE FOR S.T.I.
C.N.R.C.
MAY 30 1990
C.N.R.C.
INSTITUT CANADIEN DE L'I.S.T.

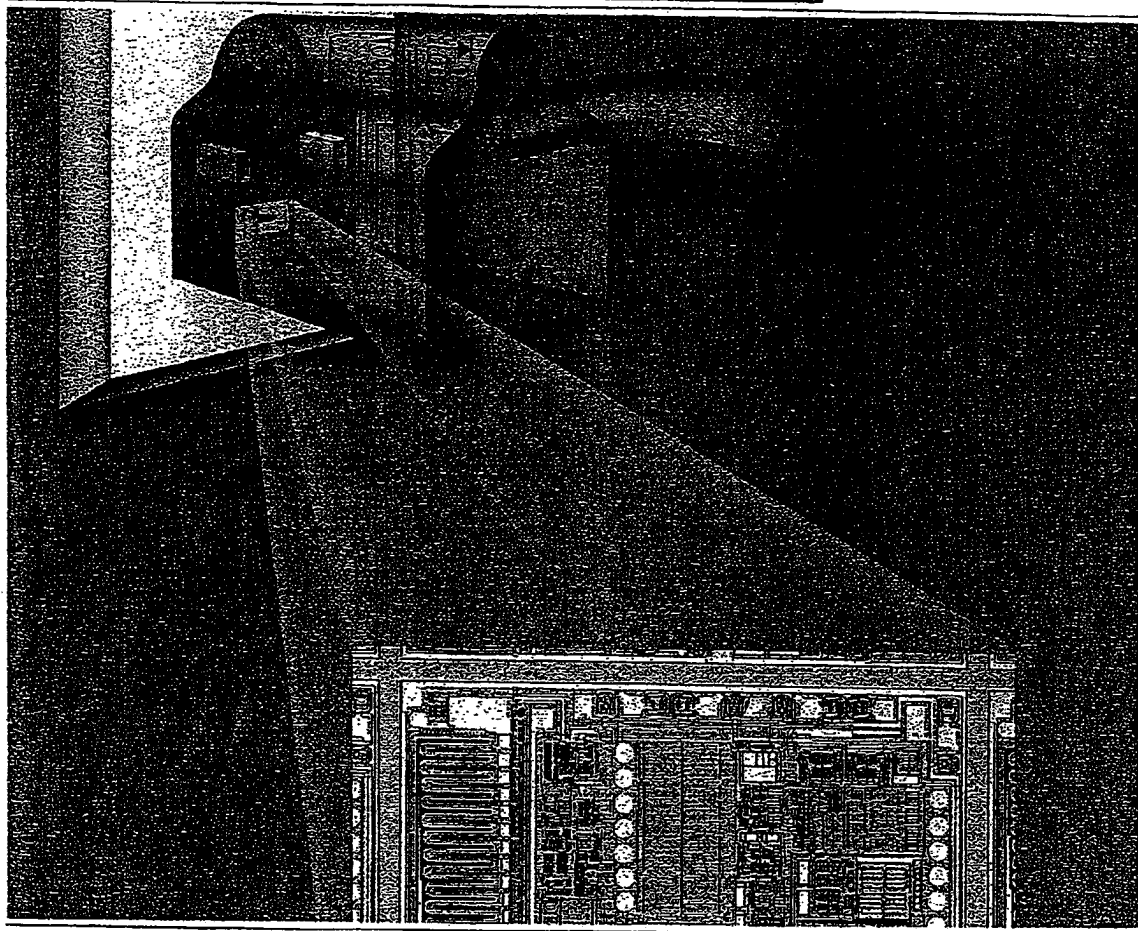
• SPECIAL REPORT: VHDL EMERGES AS A STANDARD

Case No. 04-1371-JJF
DEFT Exhibit No. DX 17
Date Entered _____
Signature _____

FCS1692104

MARCH 22, 1990 VOL. 38, NO. 6

ELECTRONIC DESIGN



COVER FEATURE

35 OFF-LINE REGULATOR HANDLES 3 W

Adding a transformer and other passive parts to a power IC creates an off-line 3-W switcher that fits into a standard wall plug.

ELECTRONIC DESIGN REPORT

45 VHDL: AN EMERGING EDA STANDARD

Despite backing by the DOD and IEEE, VHDL faces obstacles in industry-wide acceptance.

DESIGN APPLICATIONS

67 NOT TONIGHT, DARLINGTON

A two-stage dc power switch, instead of the Darlington connection, cuts costs and boosts reliability.

79 NEURAL NETWORKS DETECT SPEECH

Automating the design process is the key to neural-net systems that detect speech in the face of noise.

95 BUS MASTERS BOOST PERFORMANCE

When dealing with new buses, such as EISA and MCA, the concept of bus masters should be understood.

PRODUCT INNOVATIONS

119 MODEM ICs TRANSFER DATA, GRAPHICS

Integrated mixed-signal circuits form a data pump for high-speed, two-way data and facsimile transmission for PCs and laptops.

125 SIMPLIFY MULTIPROCESSOR DESIGN

A five-chip family gives designers a running start when building systems with multiple parallel processors.

132 SMALL ASIC TESTER HAS BIG FEATURES

A new ASIC verifier packs many capabilities of high-end production testers into a benchtop instrument.

14 EDITORIAL**19 TECHNOLOGY BRIEFING**
STD: Alive and kicking**21 TECHNOLOGY NEWSLETTER**

- BiCMOS CPU and new chips bolster Sparc family
- Tungsten deposition works under 1 micron
- Hot-atom chemistry shrinks conductive ink
- 40-pin DIP houses r-d converter trio
- Silicon dioxide makes better microwave cables
- Reduced feature set trims 32-bit DSP cost
- Advanced chips feed the incredible shrinking PC
- Flexible laminate makes thin, low-cost PC boards

28 TECHNOLOGY ADVANCES

- Researchers strive to translate signals among HDTV standards
- Direct-write scanned laser achieves submicron lithography
- Revamped Macintosh hits workstation speed, keeps compatibility

105 IDEAS FOR DESIGN

- Timer varies display intensity
- Rid measurements of supply noise
- Take the jitter out of PLLs



Certificate of Merit
Winner, 1988
Jesse H. Neal Editorial
Achievement Awards

113 PRODUCTS NEWSLETTER

- Matched transistors share one package
- Water-tight LEDs suit many styles
- Alliance yields fast 1-Mbit SRAM
- Op amp macromodels for the cost of a call
- U.S. EEPROMs gain second source in U.K.
- CMOS SRAM fits 1 Mbit in thin pack
- Compact plasma display boasts rugged design
- Chips spot and correct errors in record time
- Data access arrangement trims system cost
- Programmed polysilicon puts more gates to work

NEW PRODUCTS

- 137 Power
Integrated switching regulator handles up to 200 W/in.³
- 141 Computer-aided Engineering
- 151 Digital ICs
- 153 Analog
- 154 Instruments
- 157 Computers & Peripherals
- 158 Computer Boards

161 NEW LITERATURE**166 INDEX OF ADVERTISERS****167 READER SERVICE CARD****COMING NEXT ISSUE**

- Special Report: New processes and new designs boost IC op-amp speeds
- Special Section: PIPS—What's new in power, interconnections, packaging, switches, and relays
- Designing with a distributed-power architecture
- Design stepper-motor drives with smart bridge circuits
- Test high-speed a-d converters with a logic timing analyzer
- The benefits of building DSP functions into ASICs
- First details on a one-chip DSP system-level IC
- A new SCSI controller moves synchronous data at 10 Mbytes/s

ELECTRONIC DESIGN (USPS 172-080; ISSN 0013-4872) is published semi-monthly by Penton Publishing Inc., 1100 Superior Ave., Cleveland, OH 44114. Paid rates for a one year subscription are as follows: \$75 U.S., \$140 Canada, \$230 International. Second-class postage paid at Cleveland, OH, and additional mailing offices. Editorial and advertising addresses: ELECTRONIC DESIGN 611 Route #46 West, Hasbrouck Heights, NJ 07604. Telephone (201) 393-6060. Facsimile (201) 393-0204.

Printed in U.S.A. Title registered in U.S. Patent Office. Copyright © 1990 by Penton Publishing Inc. All rights reserved. The contents of this publication may not be reproduced in whole or in part without the consent of the copyright owner.

Permission is granted to users registered with the Copyright Clearance Center (CCC) to photocopy any article, with the exception of those for which separate ownership is indicated on the first page of the article, provided that a base fee of \$1 per copy of the article plus \$.50 per page is paid directly to the CCC, 21 Congress St., Salem, MA 01970 (Code No. 0013-4872/90 \$1.00 + .50). Copying done for other than personal or internal reference use without the express permission of Penton Publishing, Inc. is prohibited. Requests for special permission or bulk orders should be addressed to the editor. ISSN 0013-4872 \$1.00 + .50.

For subscriber change of address and subscription inquiries, call (216) 696-7060.

POSTMASTER: Please send change of address to ELECTRONIC DESIGN, Penton Publishing Inc., 1100 Superior Ave., Cleveland, OH 44114.

COVER FEATURE

ADDING A TRANSFORMER AND OTHER PASSIVE PARTS TO A POWER IC CREATES AN OFF-LINE 3-W SWITCHER THAT FITS IN A WALL PLUG.

OFF-LINE PWM SWITCHING REGULATOR IC HANDLES 3 W

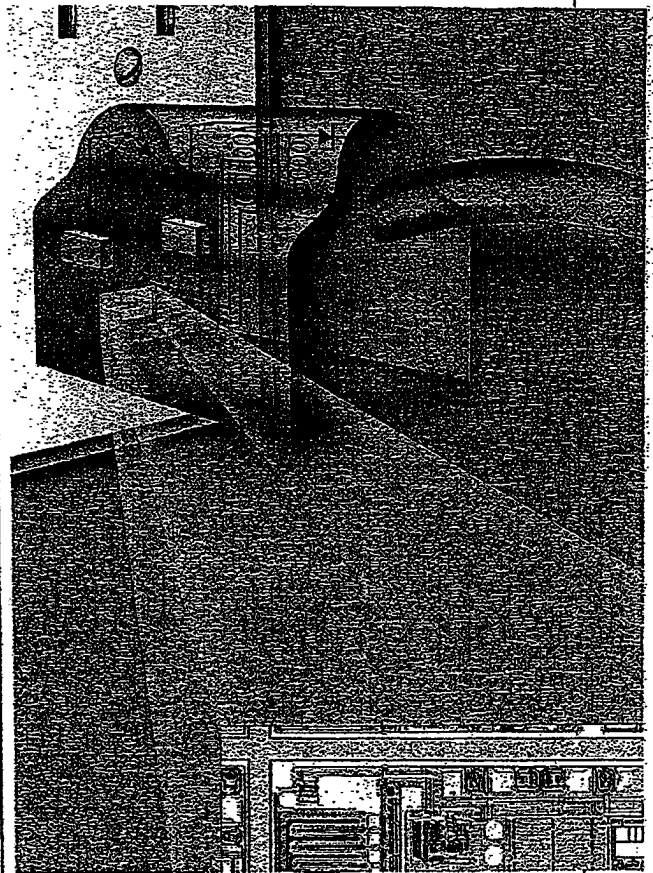
FRANK GOODENOUGH

Now you can operate a battery-powered instrument, computer, modem or other small, low-power electronic device directly from the 115-V ac line without a bulky box to plug in. All that's required is Power Integration's PWR-SMP3 regulator IC to build a 3-W isolated switching power supply. Even if a rectifier bridge and filter are included, the supply's volume can be less than 0.5 in.³ (Fig. 1). Typical cost for such a supply in high-volume quantities is between \$10 and \$20 each, depending on its size and the number built.

The PWR-SMP3 is built on the company's proprietary high-voltage CMOS process. This process puts 5-V logic and small-signal bipolar analog circuits on the same chip.

Housekeeping and/or startup circuits for large off-line supplies represent a typical application for regulators built with the PWR-SMP3. The supply can replace circuits that use bulky 115-V, 60-Hz transformers. It also lends itself to auxiliary outputs in multi-output supplies. In addition, it will simplify the design of multi-output custom circuits.

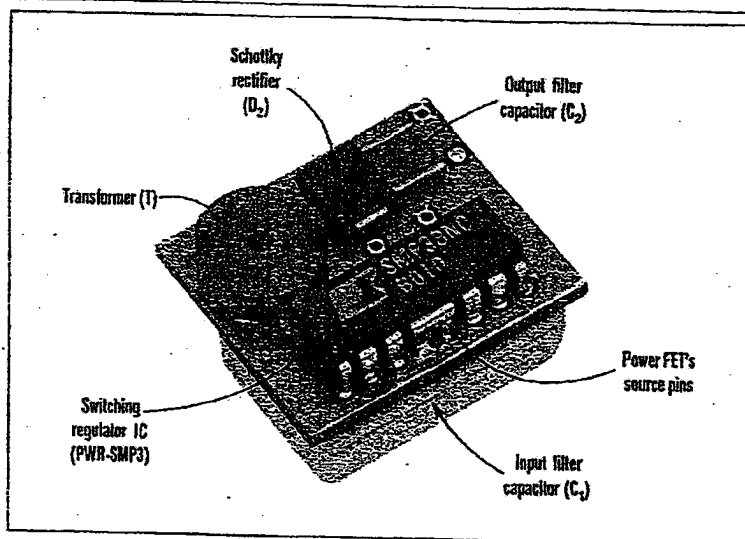
Other applications for the PWR-SMP3 include remotely located digital panel meters, credit-card readers, and remote, signal-conditioning circuits and modules. Essentially any low-power circuitry where 115 V ac is available can be powered. Because circuit voltage-isolation is a function of the transformer,



not the chip, the PWR-SMP3 can even be used in medical instrumentation or factory-floor automation systems, such as programmable controllers.

Regulators akin to the PWR-SMP3 further the trend to distributed power applications. In such applications, a relatively high voltage (50 to 200 V) is piped around a large multicabinet system to reduce IR line losses. De-to-de

COVER: OFF-LINE PWM SWITCHING REGULATOR IC



1. OCCUPYING a volume of just one-half cubic inch, this complete off-line switching regulator—built with Power Integrations PWR-SMP3 power IC in a DIP—controls up to 3 W.

converters on each system board reduce the high voltages to typical semiconductor voltage levels (see *ELECTRONIC DESIGN*, Jan. 11, p. 88). These regulators can even be smaller because the bridge rectifier and input capacitor aren't needed. With the chip's 3-W rating, supplies could be built to typically deliver 200 mA at 15 V, 250 mA at 12 V, or 600 mA at 5 V. A pair of regulators could thus supply ± 15 -V power for a slew of op amps. Or one regulator could supply 600 mA of -5.2 -V ECL power in a primarily CMOS system.

To construct a complete switching regulator, all that's required are a bridge rectifier and filter, a storage-inductor/isolation transformer, a Schottky diode, several other rectifiers and diodes, and a handful of resistors and capacitors, in addition to the PWR-SMP3 (Fig. 2). Packaged in a 16-pin DIP, the regulator is the supply's heart. Running at 1 MHz to minimize inductor size, the PWR-SMP3's controller section is optimized to implement a voltage-mode flyback circuit. Alternatively, other common pulse-width-modulated (PWM) regulator topologies may also be employed.

The chip's circuit includes all of the blocks needed for a basic PWM regulator and all of the self-protection blocks expected in today's con-

trollers (Fig. 2, again). The input dc voltage (200 V maximum) is applied to the CMOS power FET through the transformer and to a linear preregulator which drops it to the 6-V V_S required to run the control circuits during startup. Once the supply is up and running, the preregulator is turned off. The small-signal circuits on the chip are then powered from the "bootstrap"/feedback output from the transformer through the rectifier-filter formed by diode D_2 and capacitor C_2 .

Bypass capacitor C_3 keeps switching noise out of the control circuitry. Diodes D_3 and D_4 snub Ldi/dt transients as the switch turns off. A fast, low-loss Schottky diode— D_2 —rectifies the voltage across the isolated output winding of the transformer, which is filtered by C_2 to give 600 mA of regulated 5-V power. Virtually any other voltage can be generated by changing the secondary winding of the transformer.

The basic PWM circuit is conventional. The 0-to-50% duty-cycle pulses from the oscillator turn on the FET switch through the NAND-gate and the FET-gate driver. The sawtooth (ramp) output of the oscillator runs to the PWM comparator which receives its other input from the output of the error amplifier (the output is a function of the difference be-

tween the supply's output voltage through the feedback path and the output of the 1.25-V bandgap reference). When the level of the ramp reaches the output of the error amplifier, the comparator flips and turns off the FET switch through the OR gate, PWM latch, NAND gate, and driver.

NO SELF-DESTRUCT

As noted earlier, the chip is loaded with self-protection features. To start, the FET switch is a sense, or mirror, FET, with an output that feeds a small fraction of the total drain current through an on-chip current-sensing resistor, R_{sense} . The voltage developed across the resistor is applied to the current-limit comparator. When the drain current exceeds approximately 300 mA, the FET is quickly turned off.

When using this technique, voltage noise can be a problem because typical sense voltages run as low as 200 and 500 mV. Increasing the sense voltage tends to degrade the linear relationship between it and drain current. In this FET, however, proprietary compensation techniques raise the sense voltage while maintaining linearity.

On the input side of the chip, overvoltage and undervoltage (OV/UV) lockout circuits ensure that the input voltage and the 6-V internal (bias) supply are within the required limits before the supply will operate. Input OV lockout is particularly useful in off-line applications where surges or high-energy spikes are apt to be present. The supply shuts down during the transient and starts up when the input returns to the proper range. The OV/UV levels are programmed by the divider formed by resistors R_1 and R_2 . Shutdown also occurs when the internal bias voltage is too low for proper circuit operation. Hysteresis in these circuits ensures reliable, noise-free operation. The chip can either be shut down or kept from turning on by holding the OV/UV pin low. Turn-on can be delayed—for example, if turn-on of multiple supplies must be sequenced—by hanging a capacitor on the pin.

Typical UV lockout values for the

COVER: OFF-LINE PWM SWITCHING REGULATOR IC

PWR-SMP3 regulator IC are 4.6 V for the trip voltage and 4.8 V for the reset voltage. Input UV turn-off and trip-off voltages are 0.4 and 0.35 V, respectively; input OV trip-off and turn-on voltages are 1.27 and 1.21 V, respectively.

The soft-start circuit consists of a current source and an internal capacitor connected to an intermediate stage of the error amplifier. Until the capacitor is fully charged, the error amplifier output voltage is clamped low, limiting the duty cycle and peak current of the switch during startup. Once the capacitor is fully charged, the amplifier takes over and regulates the output voltage. All shutdown and lockout modes discharge this capacitor, ensuring that the supply always starts from a known state. The over-temperature shutdown circuit turns the switch off when the chip's temperature reaches between 125° and 175°C. Built-in hysteresis makes sure the temperature drops at least 45°C before the switch comes on again.

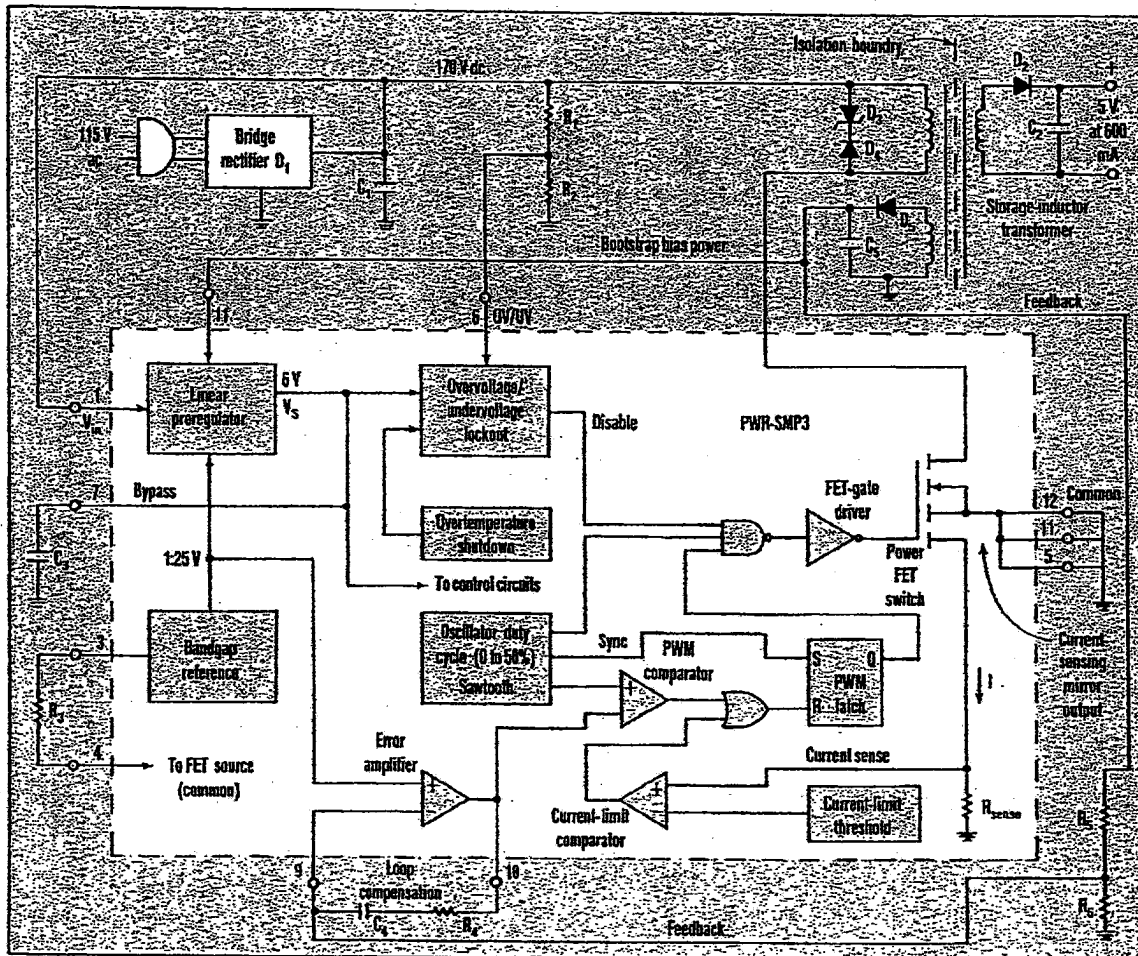
SUPERIOR CMOS

The chip will operate with input voltages between 36 and 200 V, adapting it to 48-V telecommunications applications. While oscillating at 1 MHz, the chip's quiescent current is just 4 mA. The FET switch's on-resistance is typically 14 Ω , and output capacitance is a low 8 pF. Rise and fall times of the output are typically 40 ns, with an input voltage of

160 V and a drain current of 200 mA.

In its 16-pin, plastic modified batwing package, the PWR-SMP3 can operate to 70°C. In the batwing package, which is designed to remove heat, the four center pins (4, 5, 12, and 13) are part of the copper lead frame on which the die is mounted. They're tied to the source of the FET and may be used as ground connections. Resistor R_2 is connected between pins 3 and 4 to set the internal operating currents. A separate bond wire connects pin 4 to the chip to minimize the effects of noise on the ground lines.

Power Integrations' process, in which lateral CMOS FETs are used for power switches instead of vertical DMOS FETs, brings more than



2. BY RECTIFYING AND FILTERING the 115-V ac line and applying it to the input of the PWR-SMP3 power IC through a storage-inductor/transformer, and by adding a few parts, a 5-V, 600-mA isolated and regulated PWM switching power supply can be created.

COVER: OFF-LINE PWM SWITCHING REGULATOR IC

just low cost to high- and low-voltage silicon power ICs. To start, these devices can be built on virtually any, 3.5- μ m mature CMOS line (similar to many companies, Power Integrations doesn't have a fabrication facility, so it uses multiple foundries). The 400-V FET switches from the process, comparable to so-called logic-level FETs, turn on hard with just 5 V of gate-to-source drive. This reduces gate-drive energy by a factor of four, significantly simplifying

drive circuitry (at present, discrete logic-level FETs are limited in voltage-rating to about 100 V).

Moreover, Miller capacitance at the switch's gate is usually 1/3 that of similarly rated DMOSFETs, further reducing drive energy and raising switching speeds—which reduces inductor size. Running at 1 MHz, the switch in the PWR-SMP3 takes about 1 mW of drive power, while a typical similarly rated DMOSFET uses about 20 mW.

In addition to easier drive, the positive temperature coefficient of the on-resistance of these high-voltage CMOS power FETs is less than that of similarly rated discrete MOSFETs. At 150°C, the on-resistance of a DMOSFET is 2.5 times its 25°C value, while that of the CMOS IC switch is only twice as great.

The lateral CMOS construction also makes it possible for the package's metal tab to be connected to

the source rather than to the switch's drain. This virtually eliminates displacement currents when compared with conventional technology where the drain (or collector) is connected to the case or tab.

These currents flowing through the system chassis and heat sinks contribute to system noise and common-mode electromagnetic-interference-conducted emissions. Lower noise levels may lead to less filtering to meet regulatory agency (FCC, VDE, CSA) requirements. To further increase switching speed, delays in the low-impedance driver were reduced by physically distributing the driver across the area occupied by the power FET itself. □

PRICE AND AVAILABILITY

In a 16-pin plastic DIP, the PWR-SMP3 goes for \$6 in lots of 1000. High-volume prices are significantly lower. Small quantities are available from stock.

Power Integrations Inc., 411 Clyde Ave., Mountain View, CA 94043; Art Furry or Doyle Slack, (415) 960-3572. CIRCLE 511

HOW VALUABLE?

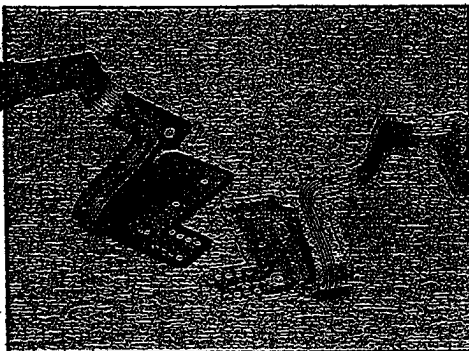
CIRCLE

HIGHLY	553
MODERATELY	534
SLIGHTLY	555

Low Cost Laminates for Static Flex Applications are Just Around the Bend.

Design your static flex circuit with polyimide film and you're on the right track, but going in the wrong direction. Polyimide film static flex circuits are expensive and can't withstand autoinsertable component mounting without the addition of rigidizers.

Design it with BEND/flex® bendable circuit laminate material from Rogers and you can realize substantial savings in material and fabrication costs. Without sacrificing design flexibility or performance. In some applications, BEND/flex laminates



BEND/flex laminates save costs compared to polyimide film circuitry.

can actually increase overall product performance.

The future belongs to designers who can think small and save big. BEND/flex laminates can help make that happen.

For all the ways BEND/flex laminates can improve your design options write for a free test kit.

Technology for tomorrow built on TQC today.

ROGERS

Rogers Corporation
Composite Materials Division
One Technology Drive
Rogers, CT 06263
203 774-9605 FAX 203 774-1973

U.L. 94V0 flame class rating.

BEND/flex is a registered trademark of Rogers Corporation. Also available through Maktron Europe, Ghent Belgium and Rogers Inoue Corp., Nagoya, Japan.

CIRCLE 97

ELECTRONIC DESIGN 39
MARCH 22, 1990

FCS1692110

FEATURE

ADDING A TRANSFORMER AND OTHER PASSIVE PARTS TO A POWER IC CREATES AN OFF-LINE 3-W SWITCHER THAT FITS IN A WALL PLUG.

OFF-LINE PWM SWITCHING REGULATOR IC HANDLES 3 W

FRANK GOODENOUGH

Now you can operate a battery-powered instrument, computer, modem or other small, low-power electronic device directly from the 115-V ac line without a bulky box to plug in. All that's required is Power Integration's PWR-SMP3 regulator IC to build a 3-W isolated switching power supply. Even if a rectifier bridge and filter are included, the supply's volume can be less than 0.5 in.³ (Fig. 1). Typical cost for such a supply in high-volume quantities is between \$10 and \$20 each, depending on its size and the number built.

The PWR-SMP3 is built on the company's proprietary high-voltage CMOS process. This process puts 5-V logic and small-signal bipolar analog circuits on the same chip.

Housekeeping and/or startup circuits for large off-line supplies represent a typical application for regulators built with the PWR-SMP3. The supply can replace circuits that use bulky 115-V, 60-Hz transformers. It also lends itself to auxiliary outputs in multi-output supplies. In addition, it will simplify the design of multi-output custom circuits.

Other applications for the PWR-SMP3 include remotely located digital panel meters, credit-card readers, and remote, signal-conditioning circuits and modules. Essentially any low-power circuitry where 115 V ac is available can be powered. Because circuit voltage-isolation is a function of the transformer,



not the chip, the PWR-SMP3 can even be used in medical instrumentation or factory-floor automation systems, such as programmable controllers.

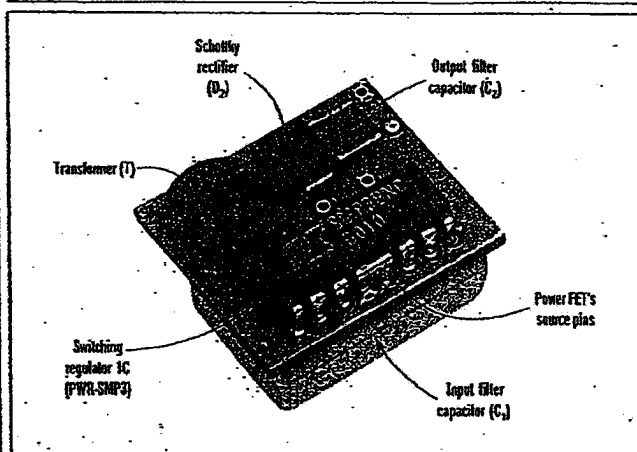
Regulators akin to the PWR-SMP3 further the trend to distributed power applications. In such applications, a relatively high voltage (50 to 200 V) is piped around a large multicabinet system to reduce IR line losses. Dc-to-dc

ELECTRONIC DESIGN 35
MARCH 22, 1990

FCS0525776

FCS1692111

COVER: OFF-LINE PWM SWITCHING REGULATOR IC



1. OCCUPYING a volume of just one-half cubic inch, this complete off-line switching regulator—built with Power Integrations PWR-SMP3 power IC in a DIP—controls up to 3 W.

converters on each system board reduce the high voltages to typical semiconductor voltage levels (see *ELECTRONIC DESIGN*, Jan. 11, p. 88). These regulators can even be smaller because the bridge rectifier and input capacitor aren't needed. With the chip's 3-W rating, supplies could be built to typically deliver 200 mA at 15 V, 250 mA at 12 V, or 600 mA at 5 V. A pair of regulators could thus supply ± 15 -V power for a slew of op amps. Or one regulator could supply 600 mA of -5.2 -V ECL power in a primarily CMOS system.

To construct a complete switching regulator, all that's required are a bridge rectifier and filter, a storage inductor/isolation transformer, a Schottky diode, several other rectifiers and diodes, and a handful of resistors and capacitors, in addition to the PWR-SMP3 (Fig. 2). Packaged in a 16-pin DIP, the regulator is the supply's heart. Running at 1 MHz to minimize inductor size, the PWR-SMP3's controller section is optimized to implement a voltage-mode flyback circuit. Alternatively, other common pulse-width-modulated (PWM) regulator topologies may also be employed.

The chip's circuit includes all of the blocks needed for a basic PWM regulator and all of the self-protection blocks expected in today's con-

trollers (Fig. 2, again). The input dc voltage (200 V maximum) is applied to the CMOS power FET through the transformer and to a linear preregulator which drops it to the 6-V V_s required to run the control circuits during startup. Once the supply is up and running, the preregulator is turned off. The small-signal circuits on the chip are then powered from the "bootstrap"/feedback output from the transformer through the rectifier-filter formed by diode D_s and capacitor C_s .

Bypass capacitor C_2 keeps switching noise out of the control circuitry. Diodes D_2 and D_1 snub Ldi/dt transients as the switch turns off. A fast, low-loss Schottky diode— D_2 —rectifies the voltage across the isolated output winding of the transformer, which is filtered by C_2 to give 600 mA of regulated 5-V power. Virtually any other voltage can be generated by changing the secondary winding of the transformer.

The basic PWM circuit is conventional. The 0-to-50% duty-cycle pulses from the oscillator turn on the FET switch through the NAND-gate and the FET-gate driver. The sawtooth (ramp) output of the oscillator runs to the PWM comparator which receives its other input from the output of the error amplifier (the output is a function of the difference be-

tween the supply's output voltage through the feedback path and the output of the 1.25-V bandgap reference). When the level of the ramp reaches the output of the error amplifier, the comparator flips, and turns off the FET switch through the OR gate, PWM latch, NAND gate, and driver.

NO SELF-DESTRUCT

As noted earlier, the chip is loaded with self-protection features. At start, the FET switch is a sense mirror, FET with an output that feeds a small fraction of the load drain current through an on-chip current-sensing resistor, R_{cs} . The voltage developed across the resistor is applied to the current limit comparator. When the drain current exceeds approximately 300 mA, the FET is quickly turned off.

When using this technique, voltage noise can be a problem because typical sense voltages run as low as 200 and 500 mV. Increasing the sense voltage tends to degrade the linear relationship between it and drain current. In this FET, however, proprietary compensation techniques raise the sense voltage while maintaining linearity.

On the input side of the chip, overvoltage and undervoltage (OV/UV) lockout circuits ensure that the input voltage and the 6-V internal (bias) supply are within the required limits before the supply will operate. Input OV lockout is particularly useful in off-line applications where surges or high-energy spikes are apt to be present. The supply shuts down during the transient and starts up when the input returns to the proper range. The OV/UV levels are programmed by the divider formed by resistors R_1 and R_2 . Shutdown also occurs when the internal bias voltage is too low for proper circuit operation. Hysteresis in these circuits ensures reliable noise-free operation. The chip can then be shut down or kept from turning on by holding the OV/UV low. Turn-on can be delayed, for example, if turn-on of multiple supplies must be sequenced by having a capacitor on the pin.

Typical UV lockout values

COVER OFF-LINE PWM SWITCHING REGULATOR IC

PWR-SMP3 regulator IC are 4.6 V for the trip voltage and 4.8 V for the reset voltage. Input UV turn-off and trip-off voltages are 0.4 and 0.35 V, respectively; input OV trip-off and turn-on voltages are 1.27 and 1.21 V, respectively.

The soft-start circuit consists of a current source and an internal capacitor connected to an intermediate stage of the error amplifier. Until the capacitor is fully charged, the error amplifier output voltage is clamped low, limiting the duty cycle and peak current of the switch during startup. Once the capacitor is fully charged, the amplifier takes over and regulates the output voltage. All shutdown and lockout modes discharge this capacitor, ensuring that the supply always starts from a known state. The over-temperature shutdown circuit turns the switch off when the chip's temperature reaches between 125°C and 175°C. Built-in hysteresis makes sure the temperature drops at least 45°C before the switch comes on again.

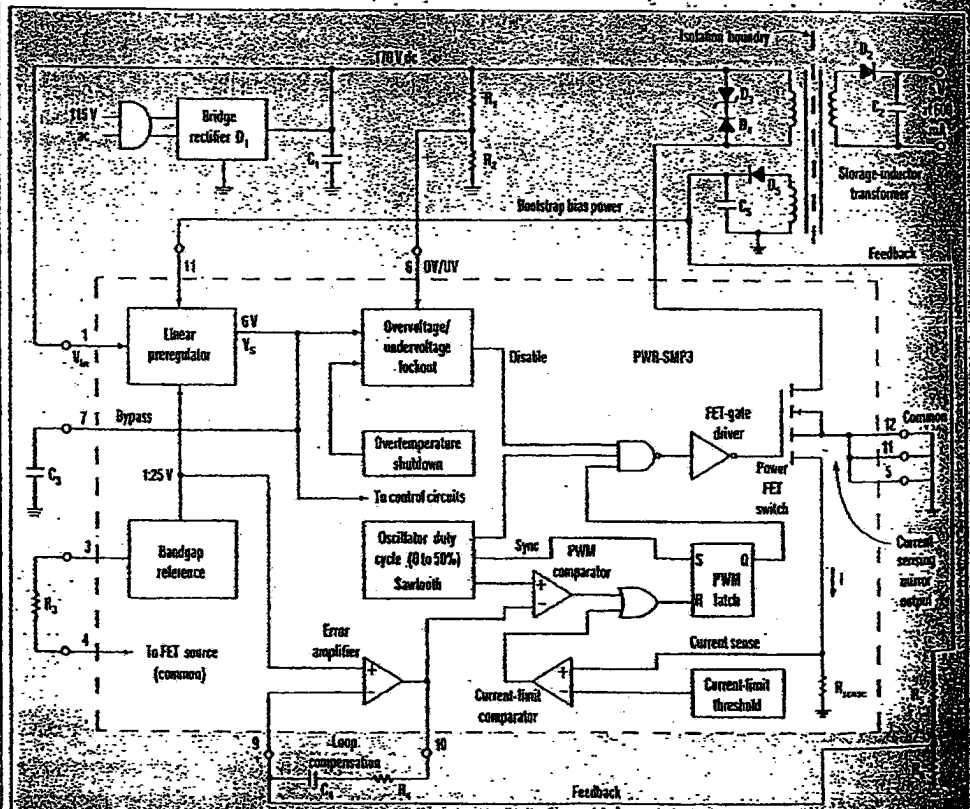
SUPERIOR CMOS

The chip will operate with input voltages between 36 and 200 V, adapting it to 48-V telecommunications applications. While oscillating at 1 MHz, the chip's quiescent current is just 4 mA. The FET switch's on-resistance is typically 14 Ω , and output capacitance is a low 8 pF. Rise and fall times of the output are typically 40 ns, with an input voltage of

160 V and a drain current of 200 mA.

In its 16-pin, plastic modified batwing package, the PWR-SMP3 can operate to 70°C. In the batwing package, which is designed to remove heat, the four center pins (4, 5, 12 and 13) are part of the copper lead frame on which the die is mounted. They're tied to the source of the FET and may be used as ground connections. Resistor R_3 is connected between pins 3 and 4 to set the internal operating currents. A separate bond wire connects pin 4 to the chip to minimize the effects of noise on the ground lines.

Power Integrations' process, in which lateral CMOS FETs are used for power switches instead of vertical DMOS FETs, brings more than



2. BY RECTIFYING AND FILTERING the 115-V ac line and applying it to the input of the PWR-SMP3 power IC (through a storage inductor/transformer, and by adding a few parts, a 5-V, 600-mA isolated and regulated PWM switching power supply can be created.

38 ELECTRONIC DESIGN
MARCH 22, 1990

FCS0525778

FCS1692113

COVER: OFF-LINE PWM SWITCHING REGULATOR IC

low cost to high- and low-voltage silicon power ICs. To start, these devices can be built on virtually any, μ m mature CMOS line (similar to many companies, Power Integrations doesn't have a fabrication facility, so it uses multiple foundries). The 400-V FET switches from the process, comparable to so-called log-level FETs, turn on hard with just 5 V of gate-to-source drive. This reduces gate-drive energy by a factor of four, significantly simplifying

drive circuitry (at present, discrete logic-level FETs are limited in voltage rating to about 100 V).

Moreover, Miller capacitance at the switch's gate is usually 1/3 that of similarly rated DMOSFETs, further reducing drive energy and raising switching speeds—which reduces inductor size. Running at 1 MHz, the switch in the PWR-SMP3 takes about 1 mW of drive power, while a typical similarly rated DMOSFET uses about 20 mW.

In addition to easier drive, the positive temperature coefficient of the on-resistance of these high-voltage CMOS power FETs is less than that of similarly rated discrete MOSFETs. At 150°C, the on-resistance of a DMOSFET is 2.5 times its 25°C value, while that of the CMOSIC switch is only twice as great.

The lateral CMOS construction also makes it possible for the package's metal tab to be connected to

the source rather than to the switch's drain. This virtually eliminates displacement currents when compared with conventional technology where the drain (or collector) is connected to the case or tab.

These currents flowing through the system chassis and heat sinks contribute to system noise and common-mode electromagnetic-interference-conducted emissions. Lower noise levels may lead to less filtering to meet regulatory agency (FCC, VDE, CSA) requirements. To further increase switching speed, delays in the low-impedance driver were reduced by physically distributing the driver across the area occupied by the power FET itself. □

PRICE AND AVAILABILITY

In a 16-pin plastic DIP, the PWR-SMP3 goes for \$6 in lots of 1000. High-volume prices are significantly lower. Small quantities are available from stock.

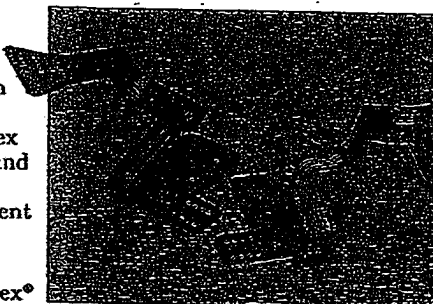
Power Integrations Inc., 411 Clyde Ave., Mountain View, CA 94043; Art Fury or Doyle Slack, (415) 960-3572. CIRCLE 511

HOW VALUABLE?	CIRCLE
HIGHLY	553
MODERATELY	554
SLIGHTLY	555

Low Cost Laminates for Static Flex Applications are Just Around the Bend.

Design your static flex circuit with polyimide film and you're on the right track, but going in the wrong direction. Polyimide film static flex circuits are expensive and can't withstand autoinsertable component mounting without the addition of rigidizers.

Design it with BEND/flex® bendable circuit laminate material from Rogers and you can realize substantial savings in material and fabrication costs. Without sacrificing design flexibility or performance. In some applications, BEND/flex laminates



BEND/flex laminates save costs compared to polyimide film circuitry.

can actually increase overall product performance.

The future belongs to designers who can think small and save big. BEND/flex laminates can help make that happen.

For all the ways BEND/flex laminates can improve your design options write for a free test kit.

Technology for tomorrow built on TQC today.

ROGERS

Rogers Corporation
Composite Materials Division
One Technology Drive
Rogers, CT 06263
203 774-9605 FAX 203 774-1973

DL 94V0 flame class rating.

BEND/flex is a registered trademark of Rogers Corporation. Also available through Mektro, Europe, Ghent Belgium and Rogers Iazac Corp., Nagoya, Japan.

CIRCLE 97

ELECTRONIC DESIGN 39
MARCH 22, 1990

FCS0525779

FCS1692114

DX 55

83CH1973-7

TECHNICAL DIGEST

ie
ma

international
**ELECTRON
DEVICES**
meeting

1983**WASHINGTON, DC****December 5-6-7**

Late News!
Page 730

Sponsored by Electron Devices Society of IEEE

Case No. 04-1371-JJF

DEFT Exhibit No. DX 55

Date Entered _____

Signature _____

FCS1692641

1983 International Electron Devices Meeting TECHNICAL DIGEST

Papers have been printed without editing as received from the authors.

All opinions expressed in the Digest are those of the authors and are not binding on The Institute of Electrical & Electronics Engineers, Inc.

Publication of a paper in this Digest in no way is intended to preclude publication of a fuller account of the paper elsewhere.

Copies of available volumes of this Digest may be obtained from The Institute of Electrical & Electronics Engineers, Inc., 445 Hoes Lane, Piscataway, N.J. Library of Congress Catalog Card Number: 78-20188.

IEEE Catalog Number: 83CH1973-7

Copyright and Reprint Permissions: Abstracting is permitted with credit to the source. Libraries are permitted to photocopy beyond the limits of U.S. copyright law for private use of patrons those articles in this volume that carry a code at the bottom of the first page, provided the per-copy fee indicated in the code is paid through the Copyright Clearance Center, 21 Congress St., Salem, MA 01970. Instructors are permitted to photocopy isolated articles for noncommercial classroom use without fee. For other copying, reprint or republication permission, write to Director, Publishing Services, IEEE, 345 E. 47 St., New York, NY 10017. All rights reserved. Copyright © 1983 by The Institute of Electrical and Electronics Engineers, Inc.

Eng/Matt
Sci LibTK
7800
I602a
1983

WELCOMING STATEMENT FROM THE GENERAL CHAIRMAN

On behalf of the conference committee I would like to welcome you to the 1983 International Electron Devices Meeting in its return to Washington, D.C. Since its inception in 1955, the IEDM has been the largest and most prestigious international forum for the presentation of the latest research and development in the area of electron devices. Last year the IEDM moved to the West Coast in order to broaden the geographical base of the meeting. This experiment was met with rousing success attracting over 2,200 attendees with a not surprisingly large component from the Bay area (1,300). In the future the meeting will be alternating between the East and West coasts to best serve both the geographically diverse US and international community of electron device researchers.

In addition to broadening its geographical base, the IEDM has also broadened its experiential base by adding panel discussions and innovations such as the author contact sessions. For the 1983 IEDM, in its 29th year, this conscious attempt to better serve the meeting attendees continues with the addition of a Sunday short course on semiconductor processing. The short course will consist of four, one and a half hour sessions, on the subjects of optical lithography, dry etching, metallization, and CVD given by renowned experts in each area. The purpose of the course is to allow those in other areas of electron device research to become acquainted with the physical basis, expected results, and equipmental capabilities for key processing techniques. It is intended that the course will provide a technical bridge to the advanced processing developments presented in the IEDM itself.

This year the IEDM contains 27 sessions in the six categories of Electron Devices, Device Technology, Integrated Circuits, Detectors, Sensors and Displays, Quantum Electronics, and Electron Tubes. These sessions contain 185 papers selected from 456 submitted abstracts from 22 countries. These statistics reflect the technical and international breadth of the meeting as well as the usual intense competition for places on the contributed program. This competition also serves to guarantee that the technical quality of the meeting remains at the high standard set by previous IEDMs and expected by the meeting attendees. In addition to the contributed papers, three areas of broad interest and relevance are highlighted in plenary session invited papers on the topics of circuit and system limitations of ultra large-scale integration, optical communications devices and systems, and visible and infrared solid-state image sensors.

Four panel discussions will also be the forum for lively debate on the topics of the extendability of CMOS technology to the submicron era, the future of silicon on insulator substrates for VLSI, device and process modeling applied to VLSI design, and optoelectronic device needs for the future.

Rounding-out the meeting will be a luncheon presentation on the topic of the Japanese 5th Generation Computer Project by Dr. Kazuhiro Fuchi, Director of the project. Dr. Fuchi will review the 5th Generation Project, a subject of intensive interest worldwide, indicating its present and future goals, present status, and placing in perspective the needs for advanced IC technology.

I would like to extend my thanks and congratulations to the Conference Committee for the outstanding job they have done in planning and organizing the 1983 IEDM and on behalf of the IEEE Electron Devices Society, which sponsors the IEDM, I want to extend my sincere appreciation for their dedicated and professional efforts.

In addition, the authors are to be commended for their efforts toward technical excellence in their papers. It is with pleasure that I welcome them and all attendees to the 1983 International Electron Devices Meeting.



Michael Adler
General Chairman



Nino Masnari
Technical Program
Chairman

Michael Adler
General Chairman

TABLE OF CONTENTS

PLENARY SESSION: Invited Papers

Monday, December 5, 9:00 a.m.
International Ballroom Center

Chairman: N. Masnari

- 1.1 VISIBLE AND INFRARED SOLID-STATE IMAGE SENSORS, W. F. Kosonocky, *RCA Laboratories, Princeton, NJ*
- 1.2 THEORETICAL, PRACTICAL AND ANALOGICAL LIMITS IN ULSI, J. D. Meindl, *Stanford University, Stanford, CA*
- 1.3 OPTICAL COMMUNICATION DEVICES AND SUBSYSTEMS, L. K. Anderson, *Bell Laboratories, Allentown, PA*

SESSION 2: Device Technology—Isolation and Dielectrics

Monday, December 5, 1:00 p.m.
International Ballroom Center

Co-Chairmen: P. Roltman
A. W. Wieder

- 1:00 p.m.
INTRODUCTION
- 1:05 p.m.
2.1 SUBMICRON MOS VLSI PROCESS TECHNOLOGIES (Invited Paper), E. Arai, *NTT ATSUGI Electrical Communication Laboratory, Kanagawa, JAPAN*
- 1:30 p.m.
2.2 CHARACTERIZATION AND MODELING OF THE TRENCH SURFACE INVERSION PROBLEM FOR THE TRENCH ISOLATED CMOS TECHNOLOGY, K. M. Cham, S. Chiang, D. Wenocur and R. D. Rung, *Hewlett-Packard Laboratories, Palo Alto, CA*
- 1:55 p.m.
2.3 A SIMPLIFIED BOX (BURIED-OXIDE) ISOLATION TECHNOLOGY FOR MEGABIT DYNAMIC MEMORIES, T. Shibata, R. Nakayama, K. Korosawa, S. Onga, M. Konaka and H. Iizuka, *Toshiba R&D Center, Kawasaki, JAPAN*
- 2:20 p.m.
2.4 CMOS TECHNOLOGY USING SEG ISOLATION TECHNIQUE, N. Endo, N. Kasai, A. Ishitani and Y. Kurogi, *NEC Microelectronics Research Labs and Fundamental Research Labs, Kawasaki, JAPAN*
- 2:45 p.m.
2.5 DEVICE ISOLATION TECHNOLOGY BY SELECTIVE LOW-PRESSURE SILICON EPITAXY, H. J. Voss and H. Kirten, *Technische Hochschule, Aachen, FEDERAL REPUBLIC OF GERMANY*
- 3:10 p.m.
2.6 A TWO-DIMENSIONAL Si OXIDATION MODEL INCLUDING VISCOELASTICITY, H. Matsumoto and M. Fukuma, *NEC Microelectronics Research Laboratories, Kawasaki, JAPAN*
- 3:35 p.m.
2.7 ENHANCED FLOW OF PHOSPHOSILICATE GLASS BY ION IMPLANTATION, D. C. Chen, R. Szeto and H. S. Fu, *Hewlett-Packard Laboratories, Palo Alto, CA*

SESSION 3: Integrated Circuits—Bipolar and CMOS Integrated Circuits

Monday, December 5, 1:00 p.m.
International Ballroom East

Co-Chairmen: K. C. Saraswat
D. D. Tang

- 1:00 p.m.
INTRODUCTION

- 1:05 p.m.
3.1 STATUS AND TRENDS OF PL/MTL TECHNOLOGY (Invited Paper), S. K. Wiedmann, *IBM, Boeblingen, FEDERAL REPUBLIC OF GERMANY* 47
- 1:30 p.m.
3.2 ADVANCED VIST DEVICE TECHNOLOGY, F. Takemoto, K. Kawakita, H. Sakai and T. Komeda, *Matsushita Electric Industrial Co., Ltd., Osaka, JAPAN* 51
- 1:55 p.m.
3.3 A NEW SELF-ALIGNED TRANSISTOR STRUCTURE FOR HIGH-SPEED AND LOW-POWER BIPOLAR LSIs, N. Ohuchi, A. Kayanuma, K. Asano, H. Hayashi and M. Noda, *SONY Corp., Atsugi, JAPAN* 55
- 2:20 p.m.
3.4 A MERGED CMOS/BIPOLAR VLSI PROCESS, F. Walczyk and J. Rubenstein, *DEC, Hudson, MA* 59
- 2:45 p.m.
3.5 A 1.0µm N-WELL CMOS/BIPOLAR TECHNOLOGY FOR VLSI CIRCUITS, I. Miyamoto, S. Saitoh, H. Momose, H. Shibata, K. Kanzaki and S. Kohyama, *Toshiba Corp., Kawasaki, JAPAN* 63
- 3:10 p.m.
3.6 SCALING OF SOI/PMOS TRANSISTORS, H. J. Singh, K. C. Saraswat, J. D. Shott, J. P. McVitte and J. D. Meindl, *Stanford University, Stanford, CA* 67

SESSION 4: Solid State Devices—Power MOS

Monday, December 5, 1:00 p.m.
International Ballroom West

Co-Chairmen: C. L. Wilson
T. Ohmi

- 23 1:00 p.m.
INTRODUCTION
- 1:05 p.m.
4.1 MODELING STATIC AND DYNAMIC BEHAVIOR OF POWER DEVICES (Invited Paper), S. Selberherr, *Technische Universität Wien, Vienna, AUSTRIA* 71
- 1:30 p.m.
4.2 A UNIFIED BIPOLAR DEVICE MODEL, G. M. Kull and L. W. Nagel, *Bell Laboratories, Murray Hill, NJ*; S. W. Lee, P. Lloyd and E. J. Prendergast, *Bell Laboratories, Allentown, PA*; H. K. Dirks, *University of Aachen, Aachen, FEDERAL REPUBLIC OF GERMANY* 75
- 1:55 p.m.
4.3 IMPROVED COMFETs WITH FAST SWITCHING SPEED AND HIGH-CURRENT CAPABILITY, A. M. Goodman, J. P. Russell, L. A. Goodman, C. J. Nuese and J. M. Neilson, *RCA Laboratories, Princeton, NJ* 79
- 2:20 p.m.
4.4 25 AMP, 500 VOLT INSULATED GATE TRANSISTORS, M. F. Chang and G. Pifer, *General Electric Co., Syracuse, NY*; B. J. Baliga, M. S. Adler and P. V. Gray, *General Electric Co., Schenectady, NY* 83
- 2:45 p.m.
4.5 OPTIMUM DESIGN OF POWER MOSFETs, P. L. Hower, T. M. S. Heng and C. Huang, *Unitrode Corp., Watertown, MA* 87
- 3:10 p.m.
4.6 1600V POWER MOSFET WITH 20ns SWITCHING-SPEED, I. Yoshida, T. Okabe and M. Nagata, *Hitachi, Tokyo, JAPAN*; T. Iijima and S. Ohtaka, *Hitachi, Gunma, JAPAN* 91
- 3:35 p.m.
4.7 EXTREMELY HIGH EFFICIENT UHF POWER MOSFET FOR HANDY TRANSMITTER, H. Itoh, *Hitachi, Gunma, JAPAN*; T. Okabe and M. Nagata, *Hitachi, Tokyo, JAPAN* 95

SESSION 5: Solid State Devices—GaAs ICs: HEMTs and Contacts

Monday, December 5, 1:00 p.m.
Jefferson Room

Co-Chairmen: R. Lee
D. K. Ferry

1:00 p.m.
INTRODUCTION

1:05 p.m.
5.1 HIGH ELECTRON MOBILITY TRANSISTORS FOR LSI CIRCUITS (Invited Paper), T. Mimura, K. Nishiuchi, M. Abe, A. Shibatomi and M. Kobayashi, *Fujitsu Limited, Atsugi, JAPAN*

1:30 p.m.
5.2 OPTIMIZATION OF HEMTS IN ULTRA HIGH SPEED GaAs INTEGRATED CIRCUITS, S. J. Lee, C. R. Crowell and C. P. Lee, *Rockwell MRDC, Thousand Oaks, CA*

1:55 p.m.
5.3 DEEP LEVEL ANALYSIS IN (AlGa) As-GaAs MODFETs BY MEANS OF LOW FREQUENCY NOISE MEASUREMENTS, L. Loreck, H. Dämbkes, K. Heime, *Universität Duisburg, FB9, Halbleitertechnik, 4100 Duisburg, FRG*; K. Ploog, *Max-Planck-Institut für Festkörperforschung, 7000 Stuttgart, FRG*

2:20 p.m.
5.4 CONTACT TECHNOLOGY IN 3-S DEVICE ANALYSIS AND MODIFICATION OF METAL-SEMICONDUCTOR CONTACT INTERFACES IN 3-S DEVICES (Invited Paper), L. J. Brillson, *Xerox, Webster, NY*

2:45 p.m.
5.5 OHMIC CONTACTS TO n-GaAs WITH GERMANIDE OVERLAYERS, S. Tiwari, T.-S. Kuan and E. Tierney, *IBM Watson Lab., Yorktown Heights, NY*

3:10 p.m.
5.6 BARRIER HEIGHTS FROM OHMIC TO BANDGAP: MODIFIED Al: GaAs SCHOTTKY DIODES BY MBE, S. J. Eglash, N. Newman, S. Pan, W. E. Spicer, D. M. Collins and M. P. Zurakowski, *Stanford and Hewlett-Packard, Palo Alto, CA*

3:35 p.m.
5.7 VIA GaAsFETs CONNECTED BY PHOTOELECTRO-CHEMICAL PLATING, L. A. D'Asaro, P. A. Kohl, C. Wolowodiuk and F. W. Ostermayer, Jr., *Bell Labs., Murray Hill, NJ*

SESSION 6: Electron Tubes—Linear Beam Devices

Monday, December 5, 1:00 p.m.
Georgetown Room

Co-Chairmen: J. Dayton
W. Wood

1:00 p.m.
INTRODUCTION

1:05 p.m.
6.1 THE CLOUDED FUTURE OF MICROWAVE TUBES AND SOLID STATE DEVICES (Invited Paper), J. T. Mendel, *Hughes Aircraft Company, Torrance, CA*

1:30 p.m.
6.2 A MILLIMETER-WAVE TUNNELADDER TWT, A. Jacques, A. Karp and A. Scott, *Varian Associates, Palo Alto, CA*

1:55 p.m.
6.3 A 30 GHz 40 WATT HELIX TRAVELING WAVE TUBE, H. Hashimoto, T. Ide, T. Konishi and R. Ohnri, *Nippon Electric Company, Ltd., Kawasaki, JAPAN*

2:20 p.m.
6.4 A CONVERGENT CONFINED-FLOW FOCUSING SYSTEM FOR MILLIMETER WAVE TUBES, J. Legarra, G. Merdianian and B. James, *Varian Associates, Palo Alto, CA*

2:45 p.m.
6.5 BONDED GRID ELECTRON GUN FOR 95 GHz EXTENDED INTERACTION AMPLIFIER, T. Grant, R. Garcia and G. Miram, *Varian Associates, Palo Alto, CA*; B. Smith, *U.S. Army Electronics Command, Ft. Monmouth, NJ*

3:10 p.m.

6.6 A 50 MEGAWATT KLYSTRON FOR THE STANFORD LINEAR COLLIDER, T. Lee, J. Lebacqz and G. Konrad, *Stanford Linear Accelerator Center, Stanford, CA*

3:35 p.m.

6.7 ION OSCILLATION CONSIDERATIONS FOR PULSED KLYSTRON AMPLIFIERS, E. McCune, *Varian Associates, Palo Alto, CA*

SESSION 7: Integrated Circuits—CMOS VLSI Device Issues

Tuesday, December 6, 9:00 a.m.
International Ballroom Center

Co-Chairmen: D. L. Fraser, Jr.
S. Kohyama

9:00 a.m.
INTRODUCTION

9:05 a.m.
7.1 DIRECTIONS IN CMOS TECHNOLOGY (Invited Paper), S. Kohyama, J. Matsunaga and K. Hashimoto, *Toshiba Corporation, Kawasaki, JAPAN*

9:30 a.m.
7.2 N-WELL AND P-WELL PERFORMANCE COMPARISON, D. Wollesen, J. Haskell and J. Yu, *Advanced Micro Devices, Inc., Sunnyvale, CA*

9:55 a.m.
7.3 COMPARISON OF LATCH-UP IN P- AND N-WELL CMOS CIRCUITS, D. Takacs, J. Harter, E. P. Jacobs, C. Werner and U. Schwabe, *Siemens AG, Munich, FEDERAL REPUBLIC OF GERMANY*; J. Winnerl and E. Lange, *Technical University Munich, Munich, FEDERAL REPUBLIC OF GERMANY*

10:20 a.m.
7.4 RESISTANCE MODULATION EFFECT DUE TO CURRENT INJECTION AND CMOS LATCHUP, Y. Nitsui, H. Nihira, K. Kanzaki and S. Kohyama, *Toshiba Corporation, Kawasaki, JAPAN*

10:45 a.m.
7.5 LATCH-UP IMMUNITY AGAINST NOISE PULSES IN A CMOS DOUBLE WELL STRUCTURE, G. Goto, H. Takahashi and T. Nakamura, *Fujitsu Laboratories Ltd., Atsugi, JAPAN*

11:10 a.m.
7.6 CHARACTERIZATION AND MODELING OF TRANSIENT LATCHUP IN CMOS TECHNOLOGY, E. Hamdy and A. Mohsen, *Intel Corporation, Aloha, OR*

*SESSION 8: Device Technology—Hot Carrier and Interface Phenomena

Tuesday, December 6, 9:00 a.m.
International Ballroom East

Co-Chairmen: D. K. Bartelink
R. B. Fair

9:00 a.m.
INTRODUCTION

9:05 a.m.
8.1 HOT-ELECTRON EFFECTS IN MOSFETs (Invited Paper), C. Hu, *University of California, Berkeley, CA*

9:30 a.m.
8.2 CHARACTERIZATION OF SIMULTANEOUS BULK AND INTERFACE HIGH-FIELD TRAPPING EFFECTS IN SiO₂, Y. Nissan-Cohen, D. Frohman-Benchkowsky and J. Shappir, *The Hebrew University, Jerusalem, ISRAEL*

9:55 a.m.
8.3 HOT-CARRIERS INDUCED DEGRADATION IN THIN GATE OXIDE MOSFETs, M.-S. Liang, C. Chang, W. Yang, C. Hu and R. W. Brodersen, *University of California, Berkeley, CA*

- 10:20 a.m.
8.4 ELECTRICAL PROPERTIES OF NITRIDED-OXIDE SYSTEMS FOR USE IN GATE DIELECTRICS AND EPROM, S. K. Lai, J. Lee and V. K. Dham, *Intel Corp., Santa Clara, CA* 190
- 10:45 a.m.
8.5 CARRIER TUNNELING RELATED PHENOMENA IN THIN OXIDE MOSFETS, C. Chang, M-S. Liang, C. Hu and R. W. Brodersen, *University of California, Berkeley, CA* 194
- 11:10 a.m.
8.6 STUDIES OF INTERFACE PHENOMENA AT SILICON GRAIN BOUNDARIES, H. C. Card, A. W. DeGroot, G. C. McGonigal, J. G. Shaw and D. J. Thomson, *University of Manitoba, Winnipeg, CANADA* 198
- 11:35 a.m.
8.7 CHARACTERIZATION OF N-CHANNEL AND P-CHANNEL LPCVD POLYSILICON MOSFETS, H. Shichijo, S. D. S. Malhi, P. K. Chatterjee, R. R. Shah, M. A. Douglas and H. W. Lam, *Texas Instruments, Dallas, TX* 202

SESSION 9: Solid State Devices—High Power Devices

Tuesday, December 6, 9:00 a.m.
Jefferson Room

Co-Chairmen: T. Ohmi
B. J. Baliga

- 9:00 a.m.
INTRODUCTION
- 9:05 a.m.
9.1 SEMICONDUCTOR CHIP DESIGN CONSTRAINTS IMPOSED BY PACKAGE LIMITATIONS (Invited Paper), C. A. Neugebauer, *General Electric Company, Schenectady, NY* 206
- 9:30 a.m.
9.2 DIRECTLY LIGHT TRIGGERED 8KV-1.2KA THYRISTOR, H. Ohashi, T. Ogura and Y. Yamaguchi, *Toshiba Research and Development Center, Kawasaki, JAPAN* 210
- 9:55 a.m.
9.3 TURN-OFF BEHAVIOR OF GTO's: 2-D NUMERICAL RESULTS COMPARED TO IR-RADIATION PATTERNS, G. Franz, *Institut für Allgemeine Elektrotechnik, Vienna, AUSTRIA*; M. Stosiek, *Siemens Research Center, Munich, FEDERAL REPUBLIC OF GERMANY* 214
- 10:20 a.m.
9.4 DETAILED COMPARISON OF EXPERIMENT AND THEORY OF PASSIVATION RING STRUCTURES FOR POWER DEVICES, D. H. Paxman and C. A. Fisher, *Phillips Research Laboratories, Surrey, ENGLAND* 218
- 10:45 a.m.
9.5 HIGH PERFORMANCE MICROWAVE STATIC INDUCTION TRANSISTORS, A. Cogan, R. Regan, I. Bencuya, S. Butler and F. Rock, *GTE Laboratories, Waltham, MA* 221
- 11:10 a.m.
9.6 A 900 MHz 100 W CW MESH EMITTER TYPE TRANSISTOR WITH P.H.S. STRUCTURE, K. Ishii, H. Yamawaki, S. Kashiwagi and E. Yamashita, *Fujitsu Discrete Semiconductor Division, Kawasaki, JAPAN* 225
- 11:35 a.m.
9.7 HIGH VOLTAGE, HIGH SPEED, GaAs SCHOTTKY POWER RECTIFIER, A. R. Sears, B. J. Baliga, P. Campbell, M. M. Barnicle and W. Garwacki, *General Electric Research and Development Center, Schenectady, NY* 229

SESSION 10: Integrated Circuits—New CAD Tools for Device Engineering

Tuesday, December 6, 9:00 a.m.
Lincoln Room

Co-Chairmen: P. Yang
E. Demoulin

9:00 a.m.
INTRODUCTION

- 9:05 a.m.
10.1 AN IGFET INVERSION CHARGE MODEL FOR VLSI SYSTEMS, L. L. Lewyn and J. D. Meindl, *Stanford University, Stanford, CA* 233
- 9:30 a.m.
10.2 AN OPTIMIZED 0.5 MICRON LDD TRANSISTOR, S. Rathnam, H. Baharansian and D. Laurent, *United Technologies/Mostek, Carrollton, TX* 237
- 9:55 a.m.
10.3 STATISTICAL MODELING FOR EFFICIENT PARAMETRIC YIELD ESTIMATION OF MOS VLSI CIRCUITS, P. Cox, P. Yang and P. Chatterjee, *Texas Instruments Inc., Dallas, TX* 242
- 10:20 a.m.
10.4 AN INTEGRATED IC PROCESS CHARACTERIZATION FACILITY (Invited Paper), D. Scharfetter, R. Tremain, T. Oki, A. Doganis and S. Chen, *Xerox Palo Alto Research Center, Palo Alto, CA* 246
- 10:45 a.m.
10.5 AN AUTOMATED METHODOLOGY FOR GENERATING SELF-CONSISTENT LAYOUT RULES FOR VLSI DESIGNS, M. Bayless, B. Waller, B. Devanney and D. Laurent, *UTC Mostek, Carrollton, TX* 250
- 11:10 a.m.
10.6 SIMPL-1 (SIMULATED PROFILES FROM THE LAYOUT-VERSION 1), M. A. Grimm, K. Lee and A. R. Neureuther, *University of California, Berkeley, CA* 255
- 11:35 a.m.
10.7 HISETS: A SOFTWARE SYSTEM FOR DESIGNING SEMICONDUCTOR DEVICE PACKAGES, A. Yasukawa, T. Sakamoto and S. Shida, *Hitachi Ltd., Tsuchiura, JAPAN* 259

SESSION 11: Electron Tubes—Gyrotrons

Tuesday, December 6, 9:00 a.m.
Georgetown Room

Co-Chairmen: R. K. Parker
J. M. Baird

- 9:00 a.m.
INTRODUCTION
- 9:05 a.m.
11.1 SURVEY OF RECENT GYROTRON DEVELOPMENTS (Invited Paper), V. L. Granatstein, *University of Maryland, College Park, MD*; S. Y. Park, *Omega-P, Inc., New Haven, CT* 263
- 9:30 a.m.
11.2 FIRST 200 kW CW OPERATION OF A 60 GHz GYROTRON, H. Jory, R. Bier, S. Evans, K. Felch, L. Fox, H. Huey, J. Shively and S. Spang, *Varian Associates, Palo Alto, CA* 267
- 9:55 a.m.
11.3 DEVELOPMENT OF 35/53 GHz GYROTRONS, T. Kageyama, I. Tsuchiya, Y. Takahashi and H. Sato, *NEC Corporation, Kawasaki, JAPAN* 271
- 10:20 a.m.
11.4 A SELF-CONSISTENT NONLINEAR ANALYSIS OF THE GYROTRON, K. Tsutaki, Y. Yuasa and Y. Morizumi, *NEC Corporation, Kawasaki, JAPAN* 273
- 10:45 a.m.
11.5 INFRARED MONITORING OF GYROTRON WINDOWS, H. Huey, N. Lopez, G. Hu, E. Choi and L. Mundie (consultant), *Varian Associates, Palo Alto, CA* 277
- 11:10 a.m.
11.6 TAPERED INTERACTION GYRO-TWA EXPERIMENTS, L. R. Barnett, *University of Utah, Salt Lake City, UT*; Y. Y. Lau and D. Dialectis, *Science Applications, McLean, VA*; K. R. Chu, *Naval Research Laboratory, Washington, DC* 280
- 11:35 a.m.
11.7 DESIGN AND OPERATION OF HIGH-HARMONIC GYROTRON OSCILLATORS AND GYRO-KLYSTRON AMPLIFIERS, D. B. McDermott, D. S. Furuno and N. C. Luhmann, Jr., *University of California, Los Angeles, CA*; P. Vitello, *Science Applications, McLean, VA* 284

SESSION 12: Quantum Electronics—Optical Sources

Tuesday, December 6, 9:00 a.m.
Thoroughbred Room

Co-Chairmen: D. Botez
J. Coleman

9:00 a.m.

INTRODUCTION

9:05 a.m.

- 12.1 VERY LOW THRESHOLD OMVPE-GROWN QUANTUM-WELL LASERS (Invited Paper), S. D. Hersee, M. Razeghi, R. Blondeau, M. Krakowski, B. deCremoux and J. P. Duchemin, *Thomson-CSF Laboratories, Orsay, FRANCE* 288

9:30 a.m.

- 12.2 TRANSVERSE-MODE STABILIZED GaAlAs LASER WITH AN EMBEDDED CONFINING LAYER ON OPTICAL GUIDE BY MOCVD, M. Okajima, Y. Muto and N. Motegi, *Toshiba Corp., Kawasaki, JAPAN* 292

9:55 a.m.

- 12.3 TEMPERATURE DEPENDENCE OF WAVELENGTH TUNING WITH SEMICONDUCTOR INTEGRATED ETALON INTERFERENCE LASERS, A. Antreasyan and S. Wang, *University of California, Berkeley, CA* 296

10:20 a.m.

- 12.4 TWISTED DOUBLE-HETEROSTRUCTURE GaAs-(AlGa)As LASER, T. Sugino and S. Wang, *University of California, Berkeley, CA* 300

10:45 a.m.

- 12.5 HIGH TEMPERATURE AND LONG LIFE OPERATION OF NEW InGaAsP/InP 1.3 μ m BURIED CRESCENT LASERS, R. Hirano, E. Oomura, H. Higuchi, Y. Sakakibara, H. Namizaki, W. Susaki and K. Fujikawa, *Mitsubishi Electric Corporation, Itami, Hyogo, JAPAN* 304

11:10 a.m.

- 12.6 ROOM TEMPERATURE PULSED OPERATION OF AlGaInP/GaInP DOUBLE HETEROSTRUCTURE VISIBLE LIGHT LASERS GROWN BY MOCVD, I. Hino, A. Gomyo, K. Kobayashi and T. Suzuki, *NEC Corporation, Kawasaki, JAPAN* 308

11:35 a.m.

- 12.7 RECENT DEVELOPMENTS IN VISIBLE LEDs, J. Nishizawa and K. Iton, *Tohoku University, Sendai, JAPAN*; Y. Okuno, F. Sakurai and M. Koike, *Semiconductor Research Institute, Sendai, JAPAN*; T. Teshima, *Stanley Electric Co., Ltd., Yokohama, JAPAN* 311

12:00 noon

- 12.8 GaAs LEDs FABRICATED ON SiO₂-COATED SI WAFERS, Y. Ohmachi, Y. Shinoda and T. Nishioka, *NTT Corp., Tokyo, JAPAN* 315

SESSION 13: Integrated Circuits—Random Access Memories

Tuesday, December 6, 2:15 p.m.
International Ballroom Center

Co-Chairpersons: L. Razouk
Y. Okuto

2:15 p.m.

INTRODUCTION

2:20 p.m.

- 13.1 A SUBMICRON CMOS MEGABIT LEVEL DYNAMIC RAM TECHNOLOGY USING DOPED FACE TRENCH CAPACITOR CELL, K. Minegishi, S. Nakajima, K. Minra, K. Harada and T. Shibata, *Nippon Telegraph and Telephone Public Corporation, Kanagawa, JAPAN* 319

2:45 p.m.

- 13.2 A 1.3 μ m n-MOS VLSI TECHNOLOGY, Y. Wada, H. Sunami, N. Yamamoto, Y. Kawamoto, T. Mizutani, K. Yagi, Y. Homma, N. Hashimoto and S. Asai, *Hitachi, Tokyo, JAPAN* 323

3:10 p.m.

- 13.3 A HIGH PERFORMANCE, HIGH DENSITY 256K DRAM UTILIZING IX PROJECTION LITHOGRAPHY, E. Adler, A. S. Bergendahl, W. Ellis, J. Fifield and E. F. O'Neill, *IBM, Essex Junction, VT* 327

3:35 p.m.

- 13.4 CIRCUIT DESIGN METHODOLOGIES, D. Segers, D. Wendell and D. Koesters, *Mostek, Carrollton, TX* 331

4:00 p.m.

- 13.5 FULLY DECODED GaAs 1Kb STATIC RAM USING CLOSELY SPACED ELECTRODE FETs, F. Katano, K. Takahashi, K. Uetake, K. Ueda, R. Yamamoto and A. Higashisaka, *NEC, Kawasaki, JAPAN* 336

4:25 p.m.

- 13.6 A 1.5 MICRON HCMOS III TECHNOLOGY FOR FAST STATIC RAMs, R. Maunel, S. Cosentino, N. Herr and J. Barnes, *Motorola, Mesa, AZ* 340

4:50 p.m.

- 13.7 SOFT ERROR RATES IN STATIC BIPOLAR RAMs, G. A. Sai-Halasz and D. D. Tang, *IBM, Yorktown Heights, NY* 344

SESSION 14: Device Technology—Silicon on Insulating Substrates

Tuesday, December 6, 2:15 p.m.
International Ballroom East

Co-Chairmen: R. Henderson
B. Griffing

2:15 p.m.

INTRODUCTION

2:20 p.m.

- 14.1 SILICON ON INSULATING SUBSTRATES—RECENT ADVANCES (Invited Paper), H. W. Lam, *Texas Instruments, Inc., Dallas, TX* 348

2:45 p.m.

- 14.2 MULTILAYER CMOS DEVICE FABRICATED ON LASER RECRYSTALLIZED SILICON ISLANDS, S. Akiyama, S. Ogawa, M. Yoneda, N. Yoshii and Y. Terui, *Matsushita Electric, Osaka, JAPAN* 352

3:10 p.m.

- 14.3 COMPARISON OF ENHANCEMENT/DEPLETION INVERTER SPEED IN BULK Si AND SOI CIRCUITS, K. K. Ng, G. W. Taylor, G. K. Celler, L. E. Trimble, R. J. Bayruns and E. I. Povelonis, *Bell Telephone Labs., Murray Hill, NJ* 356

3:35 p.m.

- 14.4 INDIRECT LASER ANNEALING OF POLYSILICON FOR THREE-DIMENSIONAL IC's, M. Nakano, R. Mukai, N. Sasaki, T. Iwai and S. Kawamura, *Fujitsu Limited, Kawasaki, JAPAN* 360

4:00 p.m.

- 14.5 3-DIMENSIONAL SOI/CMOS IC's FABRICATED BY BEAM RECRYSTALLIZATION, S. Kawamura, N. Sasaki, T. Iwai, R. Mukai, N. Nakano and M. Takagi, *Fujitsu Limited, Kawasaki, JAPAN* 364

4:25 p.m.

- 14.6 CHARACTERISTICS OF MOSFET PREPARED ON Si/MgO/Al₂O₃/SiO₂/Si STRUCTURE, Y. Hokari, M. Mikami, K. Egami, H. Tsuya and M. Kanamori, *NEC Corporation, Kanagawa, JAPAN* 368

4:50 p.m.

- 14.7 HIGH SPEED 1 μ m SOS CMOS DEVICES USING DOUBLE SOLID-PHASE EPITAXY, M. Yoshida, M. Nakahara, M. Kimura, S. Taguchi, K. Maeguchi and H. Tango, *Toshiba Corp., Kawasaki, JAPAN* 372

5:15 p.m.

- 14.8 A LOW-LEAKAGE VLSI CMOS/SOS PROCESS WITH THIN EPI LAYERS, J. Y. Lee, D. C. Mayer and P. K. Vasudev, *Hughes Research Labs., Malibu, CA* 376

SESSION 15: Solid State Devices—Low Voltage Monolithic Devices

Tuesday, December 6, 2:15 p.m.
Jefferson Room

Co-Chairmen: S. E. Diehl
D. R. Myers

2:15 p.m.

INTRODUCTION

2:20 p.m.

- 15.1 RADIATION TOLERANT DIRECT-COUPLED MISFET LOGIC ON InP, L. Messick, D. L. Lile, M. J. Taylor, C. R. Zeisse and D. A. Collins, *NOSCSan Diego, CA*; P. Pellegrini, *RADC, Hanscom AFB, MA* 380

2:45 p.m.

- 15.2 OPTIMIZED MOSFETS WITH SUBQUARTERMICRON CHANNEL LENGTHS, W. Fichtner, E. N. Fuls, R. L. Johnston, R. K. Watts and W. W. Weick, *Bell Laboratories, Murray Hill, NJ* 384

3:10 p.m.

- 15.3 SERIES RESISTANCE MODELING FOR OPTIMUM DESIGN OF LDD TRANSISTORS, C. Davvury, D. A. Baglee, M. C. Smayling and M. P. Duane, *Texas Instruments, Houston, TX* 388

3:35 p.m.

- 15.4 OPTIMIZED AND RELIABLE LDD STRUCTURE FOR $1_{\mu m}$ NMOSFET BASED ON SUBSTRATE CURRENT ANALYSIS, Y. Matsumoto, T. Higuchi, S. Sawada, S. Shinozaki and O. Ozawa, *Toshiba Corp., Kanagawa, JAPAN* 392

4:00 p.m.

- 15.5 DEVICE PERFORMANCE DEGRADATION DUE TO HOT-CARRIER INJECTION AT ENERGIES BELOW THE Si-SiO₂ ENERGY BARRIER, E. Takeda, N. Suzuki and T. Hagiwara, *Hitachi, Ltd., Tokyo, JAPAN* 396

4:25 p.m.

- 15.6 ON THE TRANSIENT AND STEADY-STATE TRANSPORT OF ELECTRONS AND HOLES IN THE MNOS AND MONOS DEVICES, A. K. Agarwal, C. Chao, R. H. Vogel and M. H. White, *Lehigh University, Bethlehem, PA* 400

4:50 p.m.

- 15.7 BIPOLAR DEVICE SCALING LIMITS FROM TUNNELING IN BASE-EMITTER JUNCTIONS, J. M. C. Stork and R. D. Isaac, *IBM, Yorktown Heights, NY* 404

SESSION 16: Solid State Devices—Integrated Power Devices

Tuesday, December 6, 2:15 p.m.
Lincoln Room

Co-Chairmen: E. Stupp
H. Strack

2:15 p.m.

INTRODUCTION

2:20 p.m.

- 16.1 INTEGRATED CIRCUITS FOR THE CONTROL OF HIGH POWER (Invited Paper), R. S. Wrathall, D. Tam, L. Terry and S. P. Robb, *Motorola, Inc., Phoenix, AZ* 408

2:45 p.m.

- 16.2 PRACTICAL SIZE LIMITS OF HIGH VOLTAGE IC's, Y. Sugawara, T. Kamei, Y. Hosokawa and M. Okamura, *Hitachi, Ltd., Ibaraki, JAPAN* 412

3:10 p.m.

- 16.3 A HIGHLY RELIABLE 16 OUTPUT HIGH VOLTAGE NMOS/CMOS LOGIC IC WITH SHIELDED SOURCE STRUCTURE, H. Wakaumi, T. Suzuki, M. Saito and H. Sakuma, *NEC Corporation, Kawasaki, JAPAN* 416

3:35 p.m.

- 16.4 LATERAL DMOS TRANSISTOR OPTIMIZED FOR HIGH VOLTAGE BIMOS APPLICATIONS, A. R. Alvarez, R. Roop, K. Ray and G. Gettemeyer, *Motorola, Inc., Mesa, AZ* 420

4:00 p.m.

- 16.5 A HIGH PERFORMANCE HIGH VOLTAGE LATERAL PNP STRUCTURE, J. D. Beason, *Harris Semiconductor, Melbourne, FL* 424

4:25 p.m.

- 16.6 EXPERIMENTAL STUDY OF A HIGH BLOCKING VOLTAGE POWER MOSFET WITH INTEGRATED INPUT AMPLIFIER, L. Leipold and J. Tihanyi, *Siemens AG, Munich, FEDERAL REPUBLIC OF GERMANY* 428

4:50 p.m.

- 16.7 A MONOLITHIC HIGH VOLTAGE SOS/CMOS OPERATIONAL AMPLIFIER, T. Kuriyama, H. Sakuma and K. Hirata, *NEC Corporation, Kawasaki, JAPAN* 432

SESSION 17: Electron Tubes—Emerging Concepts and Technologies

Tuesday, December 6, 2:15 p.m.
Georgetown Room

Co-Chairmen: J. A. Christensen
R. M. Phillips

2:15 p.m.

INTRODUCTION

2:20 p.m.

- 17.1 COMPUTERS AND TUBES—TODAY AND TOMORROW (Invited Paper), R. True, *Litton Industries, San Carlos, CA* 436

2:45 p.m.

- 17.2 IMPERIODICITY AS LIABILITY AND AS ASSET IN NON-HELIX LINEAR-BEAM TWT INTERACTION STRUCTURES, A. Karp, *Varian Associates Inc., Palo Alto, CA* 440

3:10 p.m.

- 17.3 THE DEVELOPMENT OF A NEW ANALYTICAL WAVE ANALYSIS OF A FREE ELECTRON LASER OR UBITRON, R. W. Grow, *University of Utah, Salt Lake City, UT* 444

3:35 p.m.

- 17.4 DISPENSER CATHODES: THE CURRENT STATE OF THE TECHNOLOGY, L. K. Falce, *Hughes Aircraft Company, Torrance, CA* 448

4:00 p.m.

- 17.5 THEORY OF UBITRON AMPLIFIER, A. K. Ganguly, R. K. Parker, *Naval Research Lab., Washington, DC*; H. P. Freund, *Science Applications Inc., McLean, VA*; R. H. Jackson, *Mission Research Corp., Alexandria, VA* 452

4:25 p.m.

- 17.6 DESIGN OF QUICK START, HIGH CURRENT DENSITY ELECTRON GUNS, R. C. Treseder, T. J. Grant and G. V. Miram, *Varian Associates, Palo Alto, CA* 453

4:50 p.m.

- 17.7 PROPOSING THE GYRO-PENIOTRON, WITH ITS OPERATION ANALYSIS, S. Ono, *Tohoku University*; K. Tsutaki and T. Kageyama, *NEC Corporation, Kawasaki, JAPAN* 456

SESSION 18: Quantum Electronics—III-V Heterostructure Photodetectors

Tuesday, December 6, 2:15 p.m.
Thoroughbred Room

Co-Chairmen: J. Geist
R. F. Leheny

2:15 p.m.

INTRODUCTION

2:20 p.m.

- 18.1 HIGH-SPEED InP-BASED PHOTODETECTORS (Invited Paper), F. J. Leonberger and V. Diadiuk, *Massachusetts Institute of Technology, Lexington, MA* 460

2:45 p.m.

- 18.2 HIGH-SPEED InP/InGaAsP/InGaAs AVALANCHE PHOTODIODES, J. C. Campbell, A. G. Dentai, W. S. Holden and B. L. Kasper, *Bell Laboratories, Holmdel, NJ* 464

- 3:10 p.m.
18.3 LONG WAVELENGTH, WIDE SPECTRAL RESPONSE (0.8-1.8 μ m) $\text{Al}_{0.45}\text{In}_{0.55}\text{As}/\text{Ga}_{0.47}\text{In}_{0.53}\text{As}$ AVALANCHE PHOTODIODES AND $\text{Al}_{0.45}\text{In}_{0.55}\text{As}$ ELECTROABSORPTION PIN AVALANCHE DETECTORS GROWN BY MOLECULAR BEAM EPITAXY, F. Capasso, K. Alavi, A. Y. Cho, P. W. Foy and C. G. Bethea, *Bell Laboratories, Murray Hill, NJ* 468
- 3:35 p.m.
18.4 MBE $\text{AlGa}_{1-x}\text{As}/\text{GaAs}$ PHOTOTRANSISTORS SENSITIVE AT LOW ILLUMINATION, R. Nottenburg, H. J. Buhlmann, J. C. Bischoff and M. Hegens, *Swiss Federal Inst. of Technology, Lausanne, SWITZERLAND* 472
- 4:00 p.m.
18.5 MONOLITHICALLY INTEGRATED $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ -PIN/ InP -MISFET PHOTORECEIVER, K. Kasahara, J. Hayashi, K. Makita, K. Taguchi, A. Suzuki, H. Nomura and S. Matsushita, *NEC Corporation, Kawasaki, JAPAN* 475
- 4:25 p.m.
18.6 A PLANAR EMBEDDED InGaAs PHOTODIODE ON SEMI-INSULATING InP SUBSTRATE FOR MONOLITHICALLY INTEGRATED PIN-FET RECEIVERS, USING SELECTIVE VAPOR PHASE EPITAXY AND ION IMPLANTATION TECHNIQUE, A. S. H. Liao, T. J. Bridges, E. G. Burkhardt, B. Tell, R. F. Loheny and E. D. Beebe, *Bell Laboratories, Inc., Holmdel, NJ* 478
- 4:50 p.m.
18.7 NEW OPTICAL DETECTOR USING SUPERCONDUCTING $\text{BaPb}_{0.7}\text{Bi}_{0.3}\text{O}_3$, Y. Enomoto, M. Suzuki and T. Murakami, *NTT Labs, Ibaraki, JAPAN* 482
- 5:15 p.m.
18.8 HIGH SPEED OPTICAL MODULATION WITH $\text{GaAs}/\text{GaAlAs}$ QUANTUM WELLS, T. H. Wood, D. A. B. Miller, D. S. Chemla, C. A. Burrus, T. C. Damen, A. C. Gossard and W. W. Wiegmann, *Bell Laboratories, Inc., Crawford Hill, Holmdel and Murray Hill, NJ* 486

SESSION 19: Detectors, Sensors, and Displays—Solid-State Imaging Devices

Tuesday, December 6, 2:15 p.m.
Monroe Room

Co-Chairmen: T. J. Tredwell
K. D. Wise

- 2:15 p.m.
INTRODUCTION
- 2:20 p.m.
19.1 AN 8 MEGAPIXEL/SEC 800 \times 800 VIRTUAL PHASE CCD IMAGER FOR SCIENTIFIC APPLICATIONS, R. D. McGrath and J. W. Freeman, *Texas Instruments, Dallas, TX*; J. Janesick, *Jet Propulsion Laboratory, Pasadena, CA* 489
- 2:45 p.m.
19.2 A 360,000 PIXEL COLOR IMAGE SENSOR FOR IMAGING PHOTOGRAPHIC NEGATIVES, T. J. Tredwell, T. H. Lee, B. C. Burke, T. M. Kelly, R. P. Khosla, D. L. Losee, F. C. Lo, R. L. Nielsen and W. C. McColgin, *Eastman Kodak Research Laboratories, Rochester, NY* 492
- 3:10 p.m.
19.3 A HIGH PHOTOSENSITIVITY IL-CCD IMAGE SENSOR WITH MONOLITHIC RESIN LENS ARRAY, Y. Ishihara and K. Tanigaki, *NEC Corporation, Kawasaki, JAPAN* 497
- 3:35 p.m.
19.4 BLOOMING SUPPRESSION MECHANISM FOR AN INTERLINE CCD IMAGE SENSOR WITH A VERTICAL OVERFLOW DRAIN, E. Oda, Y. Ishihara and N. Teranishi, *NEC Corporation, Kawasaki, JAPAN* 501
- 4:00 p.m.
19.5 A 3456 ELEMENT QUADRILINEAR CCD WITH DEPLETION-ISOLATED SENSOR STRUCTURE, G. Declercq, J. Bosiers, J. Sevenhans and L. Van den hove, *Katholic University, Leuven, BELGIUM* 505
- 4:50 p.m.
19.7 A NEW IMAGING DEVICE USING AMORPHOUS SILICON, C. Kusano, S. Ishioka, Y. Imamura, Y. Takasaki, Y. Shimomoto, T. Hirai and E. Maruyama, *Hitachi Ltd., Tokyo, JAPAN* 509

SESSION 20: Evening Panel Discussion

Tuesday, December 6, 8:00 p.m.
International Ballroom Center

Panel Moderator: Al F. Tasch, Jr.
Motorola
Austin, TX

SESSION 21: Evening Panel Discussion

Tuesday, December 6, 8:00 p.m.
International Ballroom East

Panel Moderators: Dimitri Antoniadis
Massachusetts Institute of Technology
Cambridge, MA
Peter Cottrell
IBM
Essex Junction, VT

SESSION 22: Evening Panel Discussion

Tuesday, December 6, 8:00 p.m.
Thoroughbred Room

Panel Moderator: Henry Kressel
E. M. Warburg, Pinus and Co.
New York, NY

SESSION 23: Evening Panel Discussion

Tuesday, December 6, 8:00 p.m.
Thoroughbred Room

Panel Moderator: Henry Kressel
E. M. Warburg, Pinus and Co.
New York, NY

SESSION 24: Device Technology—Advanced MOS Technologies

Wednesday, December 7, 9:00 a.m.
International Ballroom Center

Co-Chairmen: R. D. Davies
T. Shibata

- 9:00 a.m.
INTRODUCTION
- 9:05 a.m.
24.1 A REVIEW OF REFRACTORY GATES FOR MOS VLSI (Invited Paper), T. P. Chow, *General Electric Corp. R&D Center, Schenectady, NY*; A. J. Steckl, *Rensselaer Polytechnic Institute, Troy, NY*
- 9:30 a.m.
24.2 A HIGH PERFORMANCE CMOS TECHNOLOGY WITH TI-SILICIDED P/N-TYPE POLY-SI GATES, Y. Murao, S. Mihara, M. Kikuchi, R. Sase and T. Furuhashi, *NEC Corporation, Kanagawa, JAPAN*
- 9:55 a.m.
24.3 HIGH-SPEED LATCHUP-FREE 0.5 μ m-CHANNEL CMOS USING SELF-ALIGNED TISI, AND DEEP-TRENCH ISOLATION TECHNOLOGY, T. Yamaguchi, S. Morimoto, G. Kawamoto, H. K. Park and G. Eiden, *Tektronix Inc., Beaverton, OR*
- 10:20 a.m.
24.4 AN N-WELL CMOS WITH SELF-ALIGNED CHANNEL STOPS, J. Y. Chen, *Hughes Research Laboratories, Malibu, CA*
- 10:45 a.m.
24.5 A FULLY-SELF-ALIGNED JOINT-GATE CMOS TECHNOLOGY, A. L. Robinson, E. W. Maby and D. A. Antoniadis, *MIT, Cambridge, MA*
- 11:10 a.m.
24.6 OPTIMIZATION OF SUB-MICRON P-CHANNEL FET STRUCTURE, K. M. Cham, S.-Y. Chiang and R. D. Rung, *Hewlett-Packard Laboratories, Palo Alto, CA*

11:35 a.m.

- 24.7 **FABRICATION DEMONSTRATION OF 1-1.5 μ NMOS CIRCUITS USING OPTICAL TRI-LEVEL PROCESSING TECHNOLOGY**, K. J. Orlowsky, D. V. Speeney, E. L. Hu, J. V. Dalton and A. K. Sinha, *Bell Laboratories, Murray Hill, NJ*

SESSION 25: Device Technology—Lithography and Interconnects

Wednesday, December 7, 9:00 a.m.
International Ballroom East

Co-Chairmen: A. J. Steckl
S. Minagawa

9:00 a.m.

INTRODUCTION

9:05 a.m.

- 25.1 **MULTI-LEVEL METALLURGY FOR MASTER IMAGE STRUCTURED LOGIC** (Invited Paper), R. Geffken, *IBM Corp., Burlington, VT*

9:30 a.m.

- 25.2 **BIPOLAR PROCESS TECHNOLOGY EVALUATION BY 3-DIMENSIONAL DEVICE SIMULATION**, N. Sasaki and A. Anzai, *Hitachi Ltd., Tokyo, JAPAN*

9:55 a.m.

- 25.3 **A PLANAR METALLIZATION PROCESS—ITS APPLICATION TO TRI-LEVEL ALUMINUM INTERCONNECTION**, T. Moriya, S. Shima, Y. Hazuki, M. Chiba and M. Kashiwagi, *Toshiba R&D Center, Kawasaki, JAPAN*

10:20 a.m.

- 25.4 **VLSI PRODUCTION WITH A MULTILAYER PHOTO-LITHOGRAPHY PROCESS** (Invited Paper), G. Hillis and K. Bartlett, *Hewlett-Packard, Ft. Collins, CO*; M. Chen and R. Truina, *Hewlett-Packard, Cupertino, CA*; M. Watts, *Hewlett-Packard, Palo Alto, CA*

10:45 a.m.

- 25.5 **ELECTRON-BEAM DIRECT WRITING TECHNOLOGY FOR LSI WIRING PROCESS**, F. Murai, S. Okazaki, Y. Takeda and H. Obayashi, *Hitachi Ltd., Tokyo, JAPAN*

11:10 a.m.

- 25.6 **AN APPROACH TO QUARTER-MICRON e-BEAM LITHOGRAPHY USING OPTIMIZED DOUBLE LAYER RESIST PROCESS**, Y. Iida and S. Hasegawa, *NEC Corporation, Kawasaki, JAPAN*

11:35 a.m.

- 25.7 **SI MOSFET FABRICATION USING FOCUSED ION BEAMS**, R. L. Kubena, J. Y. Lee, R. A. Jenkins, R. G. Brauk, P. L. Middleton and E. H. Stevens, *Hughes Research Laboratories, Malibu, CA*

SESSION 26: Integrated Circuits—Non-Volatile Memory Technology

Wednesday, December 7, 9:00 a.m.
International Ballroom West

Co-Chairmen: D. C. Guterman
W. G. Oldham

9:00 a.m.

INTRODUCTION

9:05 a.m.

- 26.1 **SINGLE 5V EPROM WITH SUB-MICRON MEMORY TRANSISTOR AND ON-CHIP HIGH VOLTAGE GENERATOR**, S. Ohya, M. Kikuchi and Y. Narita, *NEC Corporation, Sagami-hara, JAPAN*

9:30 a.m.

- 26.2 **PROM CELL MADE WITH AN EPROM PROCESS**, A. Folmsbee, *Intel Corporation, Santa Clara, CA*

9:55 a.m.

- 26.3 **A NEW MASK ROM CELL PROGRAMMED BY THROUGH-HOLE USING DOUBLE POLYSILICON TECHNOLOGY**, F. Masuoka, S. Ariizumi, T. Iwase, K. Macda, M. Ono and N. Endo, *Toshiba Corporation, Saiwaiku, JAPAN*

10:20 a.m.

- 26.4 **A NEW CELL FOR HIGH CAPACITY MASK ROM BY THE DOUBLE LOCOS TECHNIQUE**, N. Sato, T. Nawata and K. Wada, *Fujitsu Limited, Nakahara, JAPAN*

10:45 a.m.

- 26.5 **HIGH TEMPERATURE AND EXTENDED ENDURANCE CHARACTERISTICS OF EEPROM**, C. S. Jeng, T. Wong and B. Joshi, *SEEQ Technology, Inc., San Jose, CA*; C. Hu, *University of California, Berkeley, CA*

11:10 a.m.

- 26.6 **DESIGN CONSIDERATIONS FOR SCALING FLOTOX E² PROM CELL**, J. Lee and V. K. Dham, *Intel Corporation, Santa Clara, CA*

11:35 a.m.

- 26.7 **OPTIMUM DESIGN OF DUAL CONTROL GATE CELL FOR HIGH DENSITY EEPROMs**, K. Hieda, M. Wada, T. Shibata, S. Inoue, M. Momodomi and H. Iizuka, *Toshiba Corporation, Kawasaki, JAPAN*

SESSION 27: Solid State Devices—III-V Devices, Characterization and Processes

Wednesday, December 7, 9:00 a.m.
Jefferson Room

Co-Chairmen: H. Goronkin
D. Ferry

9:00 a.m.

INTRODUCTION

9:05 a.m.

- 27.1 **PICOSECOND AND SUBPICOSECOND OPTOELECTRONICS FOR MEASUREMENTS OF FUTURE HIGH-SPEED ELECTRONIC DEVICES** (Invited Paper), J. Valdmantis, G. A. Mourou and C. W. Gabel, *University of Rochester, Rochester, NY*

9:30 a.m.

- 27.2 **1/f NOISE IN GaAs MESFETs**, C.-Y. Su, H. Rohdin and C. Stokte, *Hewlett-Packard Laboratories, Palo Alto, CA*

9:55 a.m.

- 27.3 **OPTIMUM PROFILES FOR LOW-NOISE ION-IMPLANTED GaAs MESFETs**, M. A. Khatibzadeh, R. J. Trew, N. A. Masnari and J. M. Golio, *North Carolina State University, Raleigh, NC*

10:20 a.m.

- 27.4 **X AND KU-BAND HIGH POWER GaAs FETs**, Y. Aono, S. Aihara and Y. Kaneko, *NEC Corporation, Kawasaki, JAPAN*

10:45 a.m.

- 27.5 **ELECTRON-BEAM FABRICATION OF QUARTER-MICRON T-SHAPED GATE FET USING A NEW TRI-LAYER RESIST SYSTEM**, P. C. Chao, P. M. Smith, S. Wanuga, J. C. M. Hwang and W. H. Perkins, *General Electric Co., Syracuse, NY*; R. Tiberio and E. D. Wolf, *Cornell University, Ithaca, NY*

11:10 a.m.

- 27.6 **PERFORMANCE AND PRINCIPLE OF OPERATION OF GaAs BALLISTIC FET**, Y. Awano, K. Tomizawa, N. Hashizume, M. Kawashima and T. Kanayama, *Electrotechnical Laboratory, Ibaraki, JAPAN*

11:35 a.m.

- 27.7 **GaAs-MESFETs WITH HIGHLY DOPED (10¹⁹CM⁻³) CHANNELS—AN EXPERIMENTAL AND NUMERICAL INVESTIGATION**, H. Dämbkes, W. Brockerhoff and K. Heime, *Universität Duisburg, Duisburg, FEDERAL REPUBLIC OF GERMANY*

12:00 p.m.

- 27.8 **InP JFETs BY SHALLOW Zn DIFFUSION**, J. B. Boos, T. H. Weng, S. C. Binari, G. Kelter and R. L. Henry, *Naval Research Laboratory, Washington, DC*

SESSION 28: Detectors, Sensors and Displays— Integrated Sensors and Sensing Devices

Wednesday, December 7, 9:00 a.m.
Lincoln Room

Co-Chairmen: S. Middelhoek
J. M. Borky

9:00 a.m.
INTRODUCTION

- 9:05 a.m.
28.1 SENSORS WITH ON-CHIP SIGNAL PROCESSING FOR LONG-TERM STABILITY (Invited Paper), J. B. Angell, Stanford University, Stanford, CA 628
- 9:30 a.m.
28.2 OFFSET REDUCTION IN A MAGNETIC-FIELD-SENSITIVE MULTICollector TRANSISTOR WITH LOW OFFSET, S. Kordic, V. Zieren and S. Middelhoek, Delft University of Technology, Delft, THE NETHERLANDS 631
- 9:55 a.m.
28.3 CARRIER TRANSPORT IN SEMICONDUCTOR MAGNETIC FIELD SENSORS, L. Andor, H. P. Baltes, A. Nathan and H. G. Schmidt-Weinmar, University of Alberta, Edmonton, Alberta, CANADA 635
- 10:20 a.m.
28.4 MONOLITHIC INTEGRATED ZINC-OXIDE ON SILICON PYROELECTRIC ANEMOMETER, D. L. Polla, R. S. Muller and R. M. White, University of California, Berkeley, CA 639
- 10:45 a.m.
28.5 REMOVING LONG TAILS FROM PHOTOCONDUCTIVE DETECTORS: A NEW MINORITY HOLE SINKED PHOTODETECTOR, C. Y. Chen, Y. M. Pang, A. Y. Cho and P. A. Garbinski, Bell Laboratories, Murray Hill, NJ 643
- 11:10 a.m.
28.6 A NEW READOUT STRUCTURE FOR RADIATION SILICON STRIP DETECTORS, W. R. Th. ten Kate and C. L. M. van der Klauw, Delft University of Technology, Delft, THE NETHERLANDS 647
- 11:35 a.m.
28.7 CHARACTERIZATION OF SURFACE AND BURIED CHANNEL ION SENSITIVE FIELD EFFECT TRANSISTORS (ISFETs), C. F. Chan and M. H. White, Lehigh University, Bethlehem, PA 651

SESSION 29: Device Technology— Process Technology

Wednesday, December 7, 1:30 p.m.
International Ballroom East

Co-Chairmen: J. Manoliu
R. R. Troutman

1:30 p.m.
INTRODUCTION

- 1:35 p.m.
29.1 COMPUTER SIMULATION IN VLSI PROCESS MODELING (Invited Paper), B. R. Penumalli, Bell Labs, Murray Hill, NJ 654
- 2:00 p.m.
29.2 MODELING RAPID THERMAL ANNEALING PROCESSES FOR SHALLOW JUNCTION FORMATION IN SILICON, R. B. Fair, MCNC, Research, Triangle Park, NC; J. J. Wortman and J. Liu, NCSU, Raleigh, NC 658
- 2:25 p.m.
29.3 RAPID-THERMAL ANNEALING OF A POLYSILICON-STACKED EMITTER STRUCTURE, N. Natsuaki, M. Tamura and T. Miyazaki, Hitachi Central Research Labs, Tokyo; Y. Yanagi, Hitachi Takasaki Works, JAPAN 662
- 2:50 p.m.
29.4 SCHOTTKY BARRIER DIODES WITH SELF-ALIGNED FLOATING GUARD RINGS, C. T. Chuang, M. Aricenzo, D. D. Tang and R. Isaac, IBM Watson Research Center, Yorktown Heights, NY 666

3:15 p.m.

- 29.5 A NEW LOW RESISTANCE SHALLOW JUNCTION FORMATION METHOD USING LATERAL DIFFUSION THROUGH SILICIDE, H. Okabayashi, E. Nagasawa and M. Morimoto, NEC Microelectronics Research Labs, Kawasaki, JAPAN 670

3:40 p.m.

- 29.6 SOURCE AND DRAIN JUNCTIONS BY OXIDIZING ARSENIC-DOPED-POLYSILICON, E. Kinsbron and W. T. Lynch, Bell Labs, Murray Hill, NJ 674

4:05 p.m.

- 29.7 NONDESTRUCTIVE EVALUATION OF GENERATION LIFETIME AND SURFACE GENERATION VELOCITY AND THE EFFECT OF ETCHING, POLISHING AND ANNEALING ON 5" SI WAFER SURFACE PROPERTIES, B. Davari, M. Tabib-Azar, K. I. Lee, F. A. Lowry and P. Das, Rensselaer Polytechnic Institute, Troy, NY; E. Mendel and D. A. Miller, IBM East Fishkill, Hopewell Junction, NY 678

Session 30: Solid State Devices—Superconducting and Novel Device Technologies

Wednesday, December 7, 1:30 p.m.
Jefferson Room

Co-Chairmen: S. M. Faris
K. Kataoka

1:30 p.m.
INTRODUCTION

- 1:35 p.m.
30.1 HIGH SPEED FOUR-BIT FULL ADDER WITH RESISTOR COUPLED JOSEPHSON LOGIC (RCJL), J. Sone, T. Yoshida and H. Abe, NEC Corporation, Kawasaki, JAPAN 682
- 2:00 p.m.
30.2 ELIMINATION OF THE EMITTER/COLLECTOR OFFSET VOLTAGE IN HETEROJUNCTION BIPOLAR TRANSISTORS, J. R. Hayes, F. Capasso, R. J. Malik, A. C. Gossard and W. Wiegmann, Bell Laboratories, Murray Hill, NJ 686
- 2:25 p.m.
30.3 DOUBLE HETEROJUNCTION GaAs-GaAlAs BIPOLAR TRANSISTORS GROWN BY MOCVD FOR EMITTER COUPLED LOGIC CIRCUITS, C. Dubon, R. Azoulay, P. Desrousseaux, J. Dangla, A. M. Duchenois, H. Hountondji and D. Ankri, Centre National D'Etudes des Telecommunications: PAB Laboratoire de Bagneux, Paris, FRANCE 689
- 2:50 p.m.
30.4 GaAsP/InGaAs SUPERLATTICE LIGHT EMITTING DIODES, M. Timmons, T. Katsuyama, R. Sillmon and S. M. Bedair, North Carolina State University, Raleigh, NC 692
- 3:15 p.m.
30.5 AN $\text{In}_{0.2}\text{Ga}_{0.8}\text{As}/\text{GaAs}$ MODULATION-DOPED, STRAINED-LAYER SUPERLATTICE FIELD-EFFECT TRANSISTOR, T. E. Zipperian, L. R. Dawson, G. C. Osborn and I. J. Fritz, Sandia National Laboratories, Albuquerque, NM 696

3:40 p.m.

- 30.6 ION-IMPLANTED STRAINED-LAYER SUPERLATTICE DEVICE, D. R. Myers, T. E. Zipperian, R. M. Biefeld and J. J. Wiczer, Sandia National Laboratories, Albuquerque, NM 700

SESSION 31: Detectors, Sensors and Displays— Infrared Detectors and Materials

Wednesday, December 7, 1:30 p.m.
Lincoln Room

Co-Chairmen: P. H. Zimmermann
P. R. Bratt

1:30 p.m.
INTRODUCTION

1:35 p.m.

- 31.1 RECENT DEVELOPMENTS IN HgCdTe PHOTOVOLTAIC DEVICES GROWN ON ALTERNATIVE SUBSTRATES USING HETEROEPITAXY (Invited Paper), W. E. Tennant, *Rockwell International Science Center, Thousand Oaks, CA*

2:00 p.m.

- 31.2 ELECTRICAL CHARACTERIZATION OF LPE N-P $\text{Hg}_{1-x}\text{Cd}_x\text{Te}/\text{CdTe}$ HETEROJUNCTIONS, P. LoVecchio, T. R. Raganath, M. N. Grimbergen, R. L. Rowe, J. D. Drake, P. H. Zimmermann and M. G. Reine, *Honeywell Electro-Optics Division, Lexington, MA*

2:25 p.m.

- 31.3 N-CHANNEL MISFETs ON LONG WAVELENGTH P- $\text{Hg}_{1-x}\text{Cd}_x\text{Te}$, R. A. Schiebel, *Texas Instruments Incorporated, Dallas, TX*

2:50 p.m.

- 31.4 ORIGIN OF NOISE CURRENTS IN ION IMPLANTED MW $\text{Hg}_{1-x}\text{Cd}_x\text{Te}$ ARRAYS, H. K. Chung and P. H. Zimmermann, *Honeywell Electro-Optics Division, Lexington, MA*

3:15 p.m.

- 31.5 DIFFUSION LIMITED DARK CURRENT IN N-TYPE $(\text{HgCd})\text{Te}$ MIS DEVICES, L. Colombo and A. J. Syllaos, *Texas Instruments Incorporated, Dallas, TX*

3:40 p.m.

- 31.6 A PISI SCHOTTKY-BARRIER INFRARED MOS AREA IMAGER WITH LARGE FILL FACTOR, M. Denda, M. Kimata, N. Yutani, N. Tsubouchi and S. Uematsu, *Mitsubishi Electric Corporation, Itami, JAPAN*

4:05 p.m.

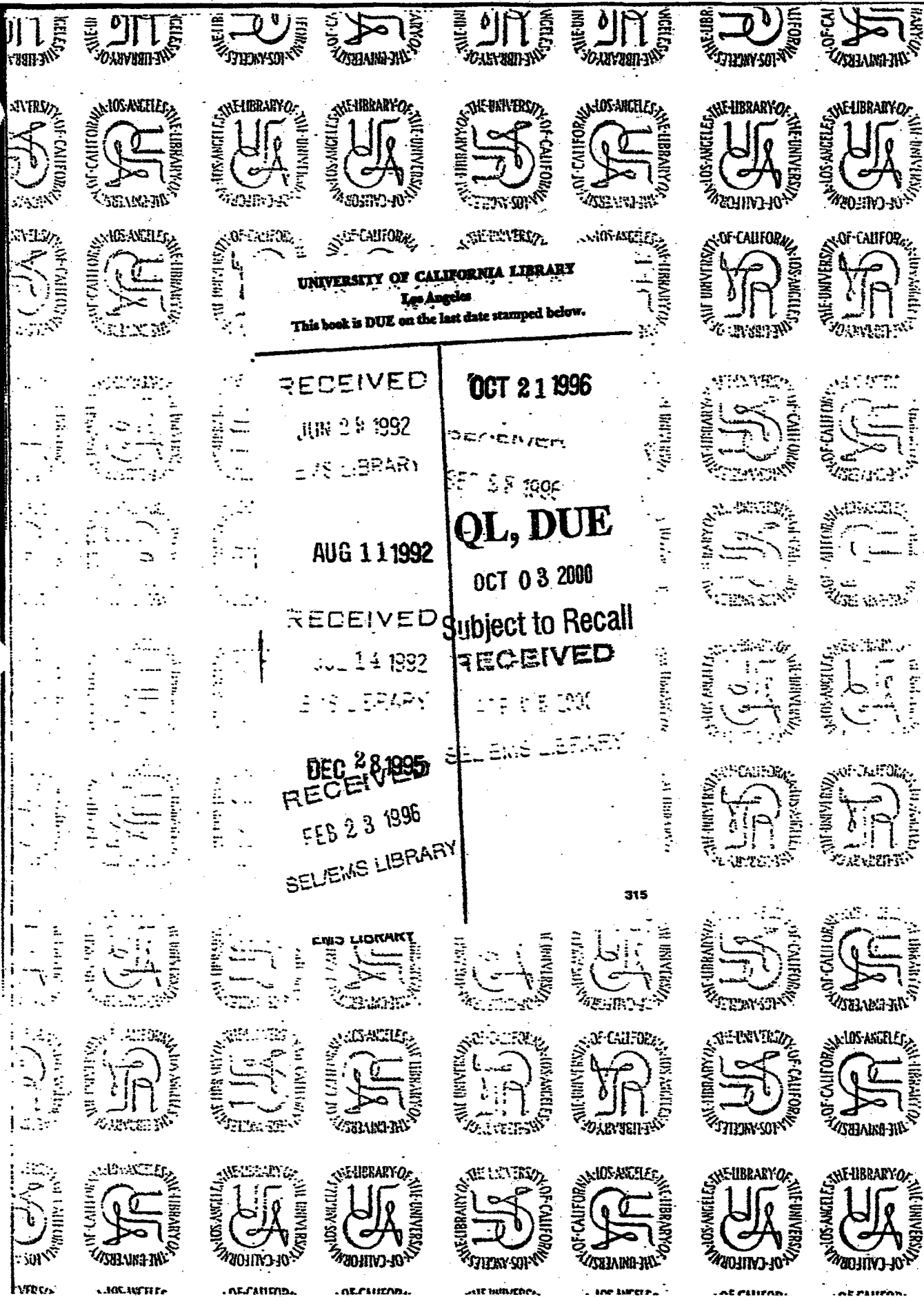
- 31.7 MONOLITHIC $128 \times 128 \text{ InSb}$ FPAs FOR STARING INFRARED IMAGING SYSTEMS, A. Bahraman and D. N. Pocock, *Northrop Research and Technology Center, Palos Verdes Peninsula, CA*

LATE NEWS

NOTE: The following paper was not available at time of publication.

4:25 p.m.

- 19.6 HIGH SPEED GaAs CCD MULTIPLEXER FOR LINEAR PHOTODETECTOR ARRAY, R. Sahai, J. Higgins, E. Sovero, R. Pierson and E. Martin, *Rockwell International, Thousand Oaks, CA*



UNIVERSITY OF CALIFORNIA LIBRARY
Los Angeles

This book is DUE on the last date stamped below.

RECEIVED

OCT 21 1996

JUN 28 1992

LIBRARY

AUG 11 1992

QL, DUE

OCT 03 2000

RECEIVED

Subject to Recall

JUN 14 1992

RECEIVED

DEC 28 1995

FEB 23 1996

SELEMS LIBRARY

315